

# First International Computer, Inc

## Portable Computer Group HW Department

Board name : MotherBoard Schematic

Project : MR040T

Version : 0.4

Initial Date : Feb. 05 , 2007

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3. Block Diagram :
4. Nat name Description :
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Manager Sign by: AVERY

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		<b>Confidential</b>	
Title: MR040T>Merom+Crestline GM965+ICH8M			
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# 1. Schematic Page Description :

## MR040T Schematic Ver : 0.1

1. Title	20. ICH8M PCI/PCIE/DMI(1/4)	39. Azalia ALC268 Codec
2. Schematic Page Description	21. ICH8M CPU/IDE/SATA(2/4)	40. AMP MAXIM9789
3. Block Diagram	22. ICH8M GPIO(3/4)	41. SPDIF / MIC / HP / Int. MIC
4. ANNOTATIONS	23. ICH8M Power/GND(4/4)	42. Mini-UMTS / BT
5. Schematic Modify	24. Reset Circuit	43. Mini-WLAN / MDC / CCD
6. Timing Diagram	25. Screw Hole	44. PMX
7. DDRII Layout Guideline	26. SPI	45. Power Block
8. Merom Processor(1/2)	27. LCD CNN	46. CPU Core Power
9. Merom Processor(2/2)	28. CRT / TVOUT CNN	47. ADPIN, BATIN, ADPOUT1
10. CPU Thermal	29. INT KB / LID / GP / SW CNN	48. Charger, DCIN
11. Crestline Host(1/6)	30. DIP SW / LED	49. 3/5VDDA/M , PMU3/5V
12. Crestline DMI/Graphic(2/6)	31. SATA & IDE CNN	50. 1.05V/1.5VDDM
13. Crestline DDRII(3/6)	32. USB CNN	51. 1.8VDDS / 0.9VDDS
14. Crestline Power(4/6)	33. Card Bus contrl	52. VDDCORE
15. Crestline Power(5/6)	34. Card Bus CNN	53. 1.25VDDM / 2.5VDDM
16. Crestline GND(6/6)	35. PCIE GIGA LAN 88E8055	54. USB Board
17. Clock Generator	36. TRANSFORMER	55. Modify list
18. DDRII SDRAM SO-DIMM0	37. Card-Reader(AU6371)	
19. DDRII SDRAM SO-DIMM1	38. IEEE1394(VIA VT6311S)	

# 2. PCI & IRQ & DMA Description :

IDSEL	CHIP
AD17	Mini PCI (Wireless LAN)
AD27	X
AD29	Lan (Realtek RTL8101L)

REQ	CHIP
REQ0 / GNT0	X
REQ1 / GNT1	LAN (Realtek RTL8101L)
REQ2 / GNT2	X
REQ3 / GNT3	X
REQ4 / GNT4	X

IRQ Channel	Description
IRQ0	System timer
IRQ1	Keyboard
IRQ2	(Casacde)
IRQ3	LAN / MODEM
IRQ4	Serial Port
IRQ5	AUDIO / VGA / USB
IRQ6	FLOPPY DISK
IRQ7	LPT
IRQ8	RTC
IRQ9	ACPI
IRQ10	FIR (Disable by default) (MODEM/LAN)
IRQ11	Cardbus
IRQ12	PS/2 mouse
IRQ13	FPU
IRQ14	HDD
IRQ15	CDROM

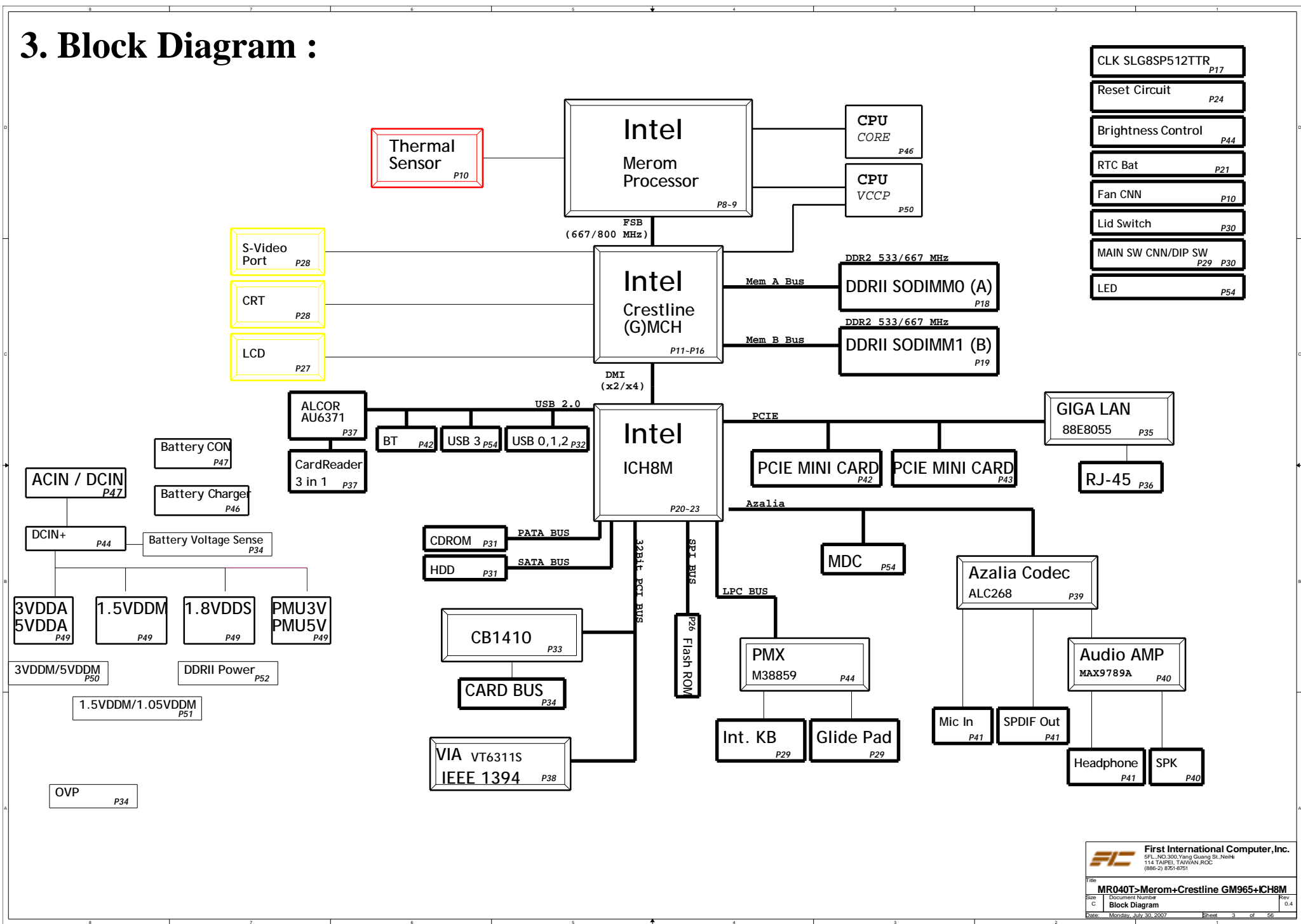
DMA Channel	Device
DMA0	FIR (disable by default) (MODEM / LAN)
DMA1	ECP
DMA2	FLOPPY DISK
DMA3	AUDIO
DMA4	(Cascade)
DMA5	Unused
DMA6	Unused
DMA7	Unused

PCIINT	CHIP
IRQA	IEEE1394 (VIA VT6311S)
IRQB	LAN (Realtek RTL8101L)
IRQC	X
IRQD	X
IRQE / GPIO2	LAN (Realtek RTL8101L)
IRQE / GPIO3	X
IRQE / GPIO4	PASS0
IRQE / GPIO5	CRISIS

20051228A



3. Block Diagram :





# 4. Nat name Description :

## Voltage Rails

DCIN	Primary DC system power supply
PMU5V	5.0V always on power rail by LATCH or ACIN
PMU3V	3.3V always on power rail by LATCH or ACIN
5VDDA	5.0V always on power rail by DCON
3VDDA	3.3V always on power rail by DCON
3VDDS	3.3V power rail by PSUSC#
5VDDS	5.0V power rail by PSUSC#
3VDDM	3.3V switched power rail by SUSTAT_B#
5VDDM	5.0V switched power rail by SUSTAT_B#
VCC_CORE	Core Voltage for CPU
1.05VDDM	1.05V power rail for AGTL+ termination/Core for GMCH by SUSTAT_B#
1.5VDDM	1.5V power rail for CPU PLL/DMI;PCIE;DDRII DLLs for GMCH/Core;PCIE for ICH7m by SUSTAT_B#
1.8VDDS	1.8V power rail for DDRII by PSUSC#
0.9VDDT_DDRII	0.9V DDRII Termination Voltage by SUSTAT_B#

## Part Naming Conventions

C	=	Capacitor
CN	=	Connector
D	=	Diode
F	=	Fuse
L	=	Inductor
Q	=	Transistor
R	=	Resistor
RP	=	Resistor Pack
U	=	Arbitrary Logic Device
Y	=	Crystal and Osc

## Net Name Suffix

#	=	Active Low signal
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# 5. Board Stack up Description

## PCB Layers

Layer 1		Component Side, Microstrip signal Layer
Layer 2		Ground Plane
Layer 3		Stripline Layer(High Speed)
Layer 4		Normal Signal / Ground 1 Plane
Layer 5		Power Plane
Layer 6		Stripline Layer(High Speed)
Layer 7		Ground 2 Plane
Layer 8		Solder Side, Microstrip signal Layer

Layers : 8 Depth 1.2mm Impence 55 ohms +/- 10%

	Single End Impedance	Differential Impedance for Microstrip	Differential Impedance for Stripline
Host Clock	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
SRC Clock	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
Host Bus	55 ohm +/- 15%		
DDR2 CLK	42 ohm +/- 15%	70 ohm +/- 20%	70 ohm +/- 20%
DDR2 Strobe	55 ohm +/- 15%		85 ohm +/- 20%
DDR2 Bus	55 ohm +/- 15%		
DMI Bus	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
PCIE Bus	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
SATA		95 ohm +/- 15%	100 ohm +/- 15%
SDVO	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
LVDS		100 ohm +/- 15%	100 ohm +/- 15%
USB		90 ohm +/- 15%	90 ohm +/- 15%
IEEE1394		110 ohm +/- 15%	110 ohm +/- 15%
Lan	50 ohm +/- 15%		



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Title

MR040T>Merom+Crestline GM965+ICH8M

Size

C

Document Number

Annotations

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6.Schematic modify Item and History :

Power Rail	Ball Name	Destination	Voltage	S0 Current
VCC_CORE		Merom HFM: LFM:	1.0375V~?~1.3000V TBD~TBD	44A TBD
1.05VDDM	VCCP VTT(VCCP) VCC VCC_PEG VCCR_RX_DMI VCC_AXM VCC1_05 VCCSUS1_05 VCCCL1_05 VCCLAN1_05	Merom: AGTL+ termination Crestline: AGTL+ termination Crestline: Core chipset Crestline: PCI Express Based Graphics Crestline: Rx and I/O Logic for DMI Crestline: Controller Link/ME voltage supply ICH8M: ICH8 Core ICH8M: ICH8M:	1.00V~1.05V~1.10V 0.9975V~1.05V~1.1025V 0.9975V~1.05V~1.1025V	4.5A 0.8A 1.3A
1.25VDDM	VCCA_SM VCCA_SM_CK VCCA_PEG_PLL VCCD_PEG_PLL VCC_DMI VCCA_HPLL VCCD_HPLL VCCA_MPLL VCCA_DPLLA VCCA_DPLLB VCC_AXG VCC_AXF VCC_DMI	Crestline: Crestline: Crestline: Crestline: Crestline: Crestline: Crestline: Crestline: Crestline: Crestline: Crestline: ICH8M:		
1.5VDDM	VCCA VCCD_QDAC VCCD_TV DAC VCCD_CRT VCCD_QDAC VCC1_5_A VCC1_5_B VCCSUS1_5 VCCGLAN1_5 VCCCL1_5 VCCUSBPLL VCCDMIPLL VCCSATAPLL VCCGLANPLL  +1.5V TBD	Merom PLL Crestline: TV DAC Crestline: TV DAC Crestline: CRT Crestline: CRT ICH8M: I/O ICH8M: I/O ICH8M: Resume well I/O ICH8M: Integrated Gigabit LAN I/O ICH8M: Controller Link ICH8M: USB PLL ICH8M: DMI PLL ICH8M: SATA PLL ICH8M: Integrated Gigabit LAN PLL  Mini Card: Express Card:	1.425V~1.5V~1.575V 1.425V~1.5V~1.575V 1.425V~1.5V~1.575V 1.425V~1.5V~1.575V 1.425V~1.5V~1.575V          1.7V~1.8V~1.9V	130mA 1.5A 60mA 24mA 320mA
1.8VDDS:	VCC_SM VCC_SM_CK VCCD_LVDS VCC_TX_LVDS VCCA_LVDS 1.8VDDS:	Crestline: I/O Voltage Crestline: Clock I/O Voltage Crestline: Crestline: Crestline: SO-DIMM:		3.1A
0.9VDDT_DDRII:		DDRII Terminator:	0.855V~0.9V~0.945V	1.0A

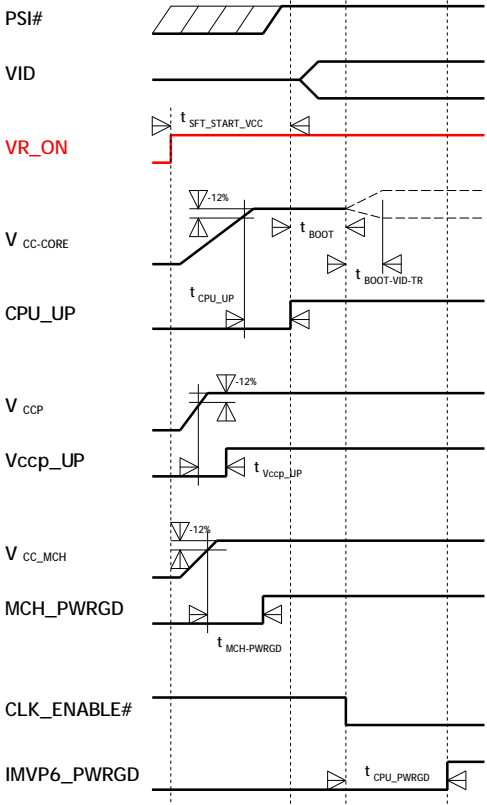
Need Modify

Power Rail	Ball Name	Destination	Voltage	S0 Current
2.5VDDM		945GM: PCIE analog 945GM: LVDS analog 945GM: LVDS I/O 945GM: CRT DAC CH7307:	2.32V~2.5V~2.625V 2.375V~2.5V~2.625V 2.375V~2.5V~2.625V 2.32V~2.5V~2.625V	2mA 10mA 60mA 70mA
3VDDM	VCCA_PEG_BG VCC_HV VCC_SYNC VCCA_CRT_DAC VCCA_TVA_DAC VCCA_TV_B_DAC VCCA_TV_C_DAC VCCA_DAC_BG	Crestline: PCI Express Base Graphics Crestline: HV buffer power Crestline: H/VSYNC power Crestline: CRT DAC Crestline: TV Out Crestline: TV Out Crestline: TV Out Crestline: TV DAC  ICH7m: Mini Card: Express Card: CLK Generator: ICS954226 KBC: KB3886 Flash ROM: BIOS Azalia Codec: ALC260 Azalia MDC: HDD: SATA	3.135V~3.3V~3.465V 3.135V~3.3V~3.465V          3.135V~3.3V~3.465V  3.0V~3.3V~3.6V	40mA 120mA          400mA
3VDDS		Lan: Broadcom BCM4401 Card Reader: SD/MMC/MS Azalia MDC: For wake up	3.0V~3.3V~3.6V	
3VDDA		ICH7m: ICH7m: ICH7m: LCD:	   3.0V~3.3V~3.6V	1.0A
5VDDM		Azalia Codec: ALC260 Azalia MDC: HDD: SATA ODD: PATA Audio AMP: G1420 Inverter:	3.0V~3.3V~3.6V  4.75V~5.0V~5.25V 4.75V~5.0V~5.25V	Max: 1.0A ; R/W Max: 1.8A ; R/W: 900mA
5VDDS		USB: x 4 ports	5V	2.0A
PMU3V		EC: PMU08 ICH7m: RTC		



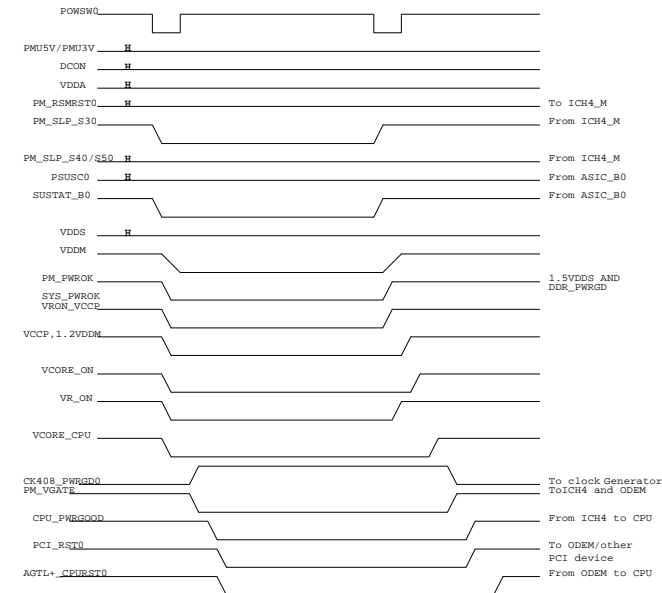
# 7. power on & off & S3 Sequence :

Power On Sequencing Timing Diagram  
20060117A - DATA FROM NO.16809

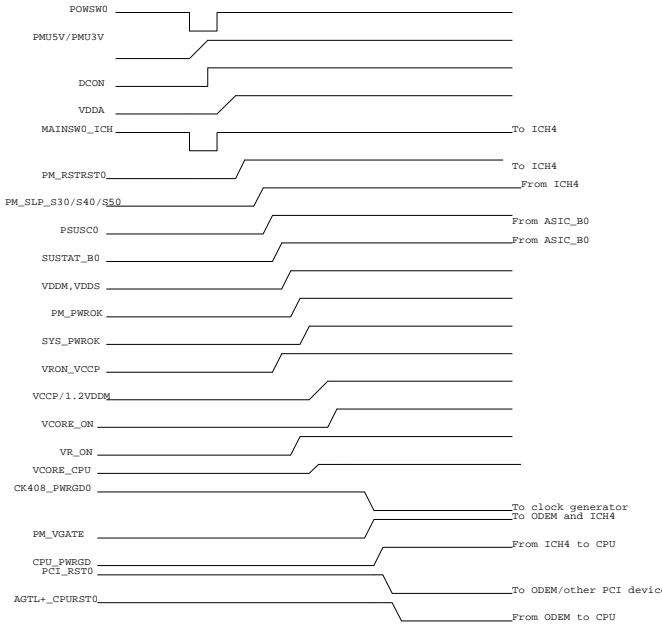


t <sub>SFT_START_VCC</sub>	Max = 3 ms
t <sub>BOOT</sub>	Min = 10 us , Max = 100 us
t <sub>BOOT-VID-TR</sub>	Max = 100 us
t <sub>CPU_UP</sub>	Min = 10 us , Max = 30 us
t <sub>Vccp_UP</sub>	Min = 10 us , Max = 30 us
t <sub>MCH-PWRGD</sub>	Min = 10 us , Max = 30 us
t <sub>CPU_PWRGD</sub>	Min = 3 ms , Max = 20 ms

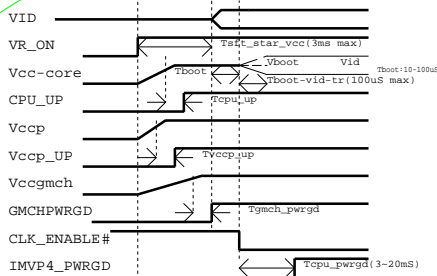
## S3 SUSPEND AND RESUME TIMING



## BATTERY ONLY POWER ON TIMING



## IMVP6 Power On Sequencing Timing Diagram





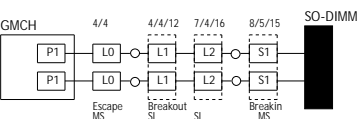
# 8. Layout Guideline :

## Crestline DDRII Layout Guidelines

### DDRII Signal Groups

Group	Signal Name	Length Matching and Length Formulas
Data	SA_DQ[63..0]/SB_DQ[63..0] SA_DM[7..0]/SB_DM[7..0] SA_DSQ[7..0]/SB_DSQ[7..0]	
Address	SA_MA[13..0]/SB_MA[13..0] SA_BS[2..0]/SB_BS[2..0] SA_RAS#/SB_RAS# SA_CAS#/SB_CAS# SA_WE#/SB_WE#	
Control	SM_CKE[3..0] SM_ODT[3..0]	
Clock	SM_CLK[3..0] SM_CK[3..0]	
FeedBack	SA_RCVENOUT#/SB_RCVENOUT# SA_RCVENIN#/SB_RCVENIN#	

### CLK group : SM\_CLK[3..0],SM\_CK[3..0]



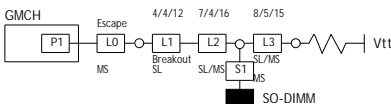
Topology	Differential Pair Point-to-Point
Reference Plane	Ground
Single Ended Trace Impedance	42 +/- 15%
Differential Mode Impedance	70 +/- 20%
Nominal Trace Width	Inner Layer : 7 mils Outer Layer : 8 mils
Nominal CK to CK# Spacing (edge to edge)	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum Serpentine Spacing	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Spacing to Other DDR2	Inner Layer : 16 mils Outer Layer : 20 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length Range - P1	1000 mils +/- 250 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1	Min = 500 mils Max = 4000 mils
Total Length - P1 + L0 + L1 + L2 + S1	Max = 4500 mils
Maximim Via Count	2 (Per side)
SCK to SCK# Length Matching (Total Length)	Match total length to within 5 mils
Clock to Clock Length Match (Total Length)	Match Channel A clocks to X0 +/- 20mils Match Channel A clocks to X1 +/- 20mils
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4/12 mils to other DDR2 Outer Layer : 5/15 mils to other DDR2 Max. breakout length is 500 mils
Breakin Exception s (Reduce geometries for SO-DIMM break-in region)	CK to CK# spacing rule waived at connector spacing of 15 mils to other DDR2 Max. breakin length is 2 00 mils

### Feedback group :

SA\_RCVENIN#],SA\_RCVENOUT#],SB\_RVENIN#],SB\_RCVENOUT#]

These signals are routed internally on the GMCH package and don't require any routing on the MB. As a result, can be left as NC.

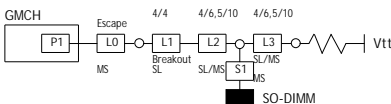
### Control group : SM\_CKE[3..0],SM\_CS#[3..0],SM\_ODT[3..0]



Topology	Point-to-Point with parallel termination
Reference Plane	Ground
Characteristic Trace Impedance	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum CTRL Trace Spacing	Inner Layer : 8 mils Outer Layer : 10 mils
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length P1	750 mils +/- 200 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 5000 mils
Trace Length L3	Max = 1500 mils
Parallel Termination Resistor	56 +/- 5%
Maximim Via Count	3
CTRL to SCK/SCK# Length Matching (Total Length including package)	(CLK-1.0") <= CTRL <= (CLK-0.0")
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4 mils spacing allowed Outer Layer : 5 mils spacing allowed Max. breakout length is 500 mils

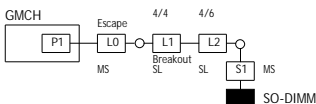
### Command group :

SA\_MA[13..0],SB\_MA[13..0],SA\_BS[2..0],SB\_BS[2..0],SA\_RAS#],SB\_RAS#],SA\_CAS#],SB\_CAS#],SA\_WE#],SB\_WE#]



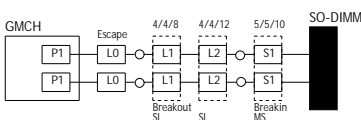
Topology	Point-to-Point with parallel termination
Reference Plane	Ground
Characteristic Trace Impedance	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum CMD Bus Trace Spacing	Inner Layer : 6 mils Outer Layer : 5 mils
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length P1	750 mils +/- 350 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 5000 mils
Trace Length L3	Max = 1500 mils
Parallel Termination Resistor	56 +/- 5%
Maximim Via Count	3
CTRL to SCK/SCK# Length Matching (Total Length including package)	(CLK-1.0") <= CMD <= (CLK+1.0")
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4 mils spacing allowed Outer Layer : 5 mils spacing allowed Max. breakout length is 500 mils

### Data group : SA\_DQ[63..0],SB\_DQ[63..0],SA\_DM[7..0],SB\_DM[7..0]



Topology	Point-to-Point
Reference Plane	Ground
Characteristic Trace Impedance	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum DQ Bus Trace Spacing	Inner Layer : 6 mils Outer Layer : 8 mils
Minimum Serpentine Spacing	Same as DQ-to-DQ routing
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length P1	750 mils +/- 350 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 5000 mils
Trace Length L3	Max = 1500 mils
Maximim Via Count	2
DQ/DM to DQS Length Matching (Total Length including package)	Match DQ/DM to (SDQS - 200mils) +/- 20mils, per byte lane
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4 mils spacing allowed Outer Layer : 5 mils spacing allowed Max. breakout length is 500 mils

### Data Strobe group : SA\_DQS[7..0],SA\_DQS#[7..0],SB\_DQS[7..0],SB\_DQS#[7..0]



Topology	Differential Pair Point-to-Point
Reference Plane	Ground
Single Ended Trace Impedance	55 +/- 15%
Differential Mode Impedance	85 +/- 20%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils
Nominal DQS to DQS# Spacing (edge to edge)	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum DQS to DQ Spacing	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Serpentine Spacing	Inner Layer : 8 mils Outer Layer : 10 mils
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length Range - P1	750 mils +/- 350 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 5000 mils
Maximim Via Count	2 (Per side)
DQS to DQS# Length Matching	Match total length to within 5 mils
Clock to Clock Length Match (Total Length include package)	(CLK-0.5") <= DQS <= (CLK+1.0")
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 8 mils to other DDR2 Outer Layer : 10 mils to other DDR2 Max. breakout length is 500 mils
Breakin Exceptions (Reduce geometries for SO-DIMM break-in region)	DQS to DQS# spacing rule waived at connector spacing of 10 mils to other DDR2 Max. breakin length is 2 00 mils







Place these inside socket cavity on L8  
(North side secondary)

Place these inside socket cavity on L8  
(South side secondary)

VCORE\_CPU

HFM  
ICC=41A

Place these inside socket cavity on L1  
(North side Primary)

Place these inside socket cavity on L1  
(South side Primary)

North side secondary

South side secondary

1.05VDDM  
ICCP=4.5A, 180mils

Place these inside socket cavity on L8  
(North side secondary)

1.5VDDM  
ICCA=130mA, 20mils

Place C?  
Close To pin  
B26

TDK

VCORE\_CPU

R117  
1000 1% 1/16W SMT0402 LR

R120  
1000 1% 1/16W SMT0402 LR

Route VCCSENSE and VSSSENSE traces at 27.4 ohms with 50mils spacing.  
Place PU and PD within 1 inch of CPU

L8B6		
A4	VSS001	VSS083
A8	VSS002	VSS084
A11	VSS003	VSS085
A14	VSS004	VSS086
A16	VSS005	VSS087
A19	VSS006	VSS088
A23	VSS007	VSS089
A27	VSS008	VSS090
B6	VSS009	VSS091
B9	VSS010	VSS092
B11	VSS011	VSS093
B13	VSS012	VSS094
B16	VSS013	VSS095
B19	VSS014	VSS096
B21	VSS015	VSS097
B24	VSS016	VSS098
C6	VSS017	VSS099
C9	VSS018	VSS100
C11	VSS019	VSS101
C14	VSS020	VSS102
C16	VSS021	VSS103
C19	VSS022	VSS104
C22	VSS023	VSS105
C25	VSS024	VSS106
D4	VSS025	VSS107
D8	VSS026	VSS108
D11	VSS027	VSS109
D13	VSS028	VSS110
D16	VSS029	VSS111
D19	VSS030	VSS112
D22	VSS031	VSS113
D25	VSS032	VSS114
E4	VSS033	VSS115
E8	VSS034	VSS116
E11	VSS035	VSS117
E14	VSS036	VSS118
E16	VSS037	VSS119
E19	VSS038	VSS120
E21	VSS039	VSS121
E24	VSS040	VSS122
F4	VSS041	VSS123
F8	VSS042	VSS124
F11	VSS043	VSS125
F13	VSS044	VSS126
F16	VSS045	VSS127
F19	VSS046	VSS128
F22	VSS047	VSS129
F25	VSS048	VSS130
G4	VSS049	VSS131
G8	VSS050	VSS132
G11	VSS051	VSS133
G14	VSS052	VSS134
G16	VSS053	VSS135
G19	VSS054	VSS136
G21	VSS055	VSS137
G24	VSS056	VSS138
H4	VSS057	VSS139
H8	VSS058	VSS140
H11	VSS059	VSS141
H13	VSS060	VSS142
H16	VSS061	VSS143
H19	VSS062	VSS144
J4	VSS063	VSS145
J8	VSS064	VSS146
J11	VSS065	VSS147
J13	VSS066	VSS148
J16	VSS067	VSS149
J19	VSS068	VSS150
J21	VSS069	VSS151
J24	VSS070	VSS152
K4	VSS071	VSS153
K8	VSS072	VSS154
K11	VSS073	VSS155
K13	VSS074	VSS156
K16	VSS075	VSS157
K19	VSS076	VSS158
L4	VSS077	VSS159
L8	VSS078	VSS160
L11	VSS079	VSS161
L13	VSS080	VSS162
L16	VSS081	VSS163



The diagram shows a detailed PCB layout for a thermal sensor. Key components include:

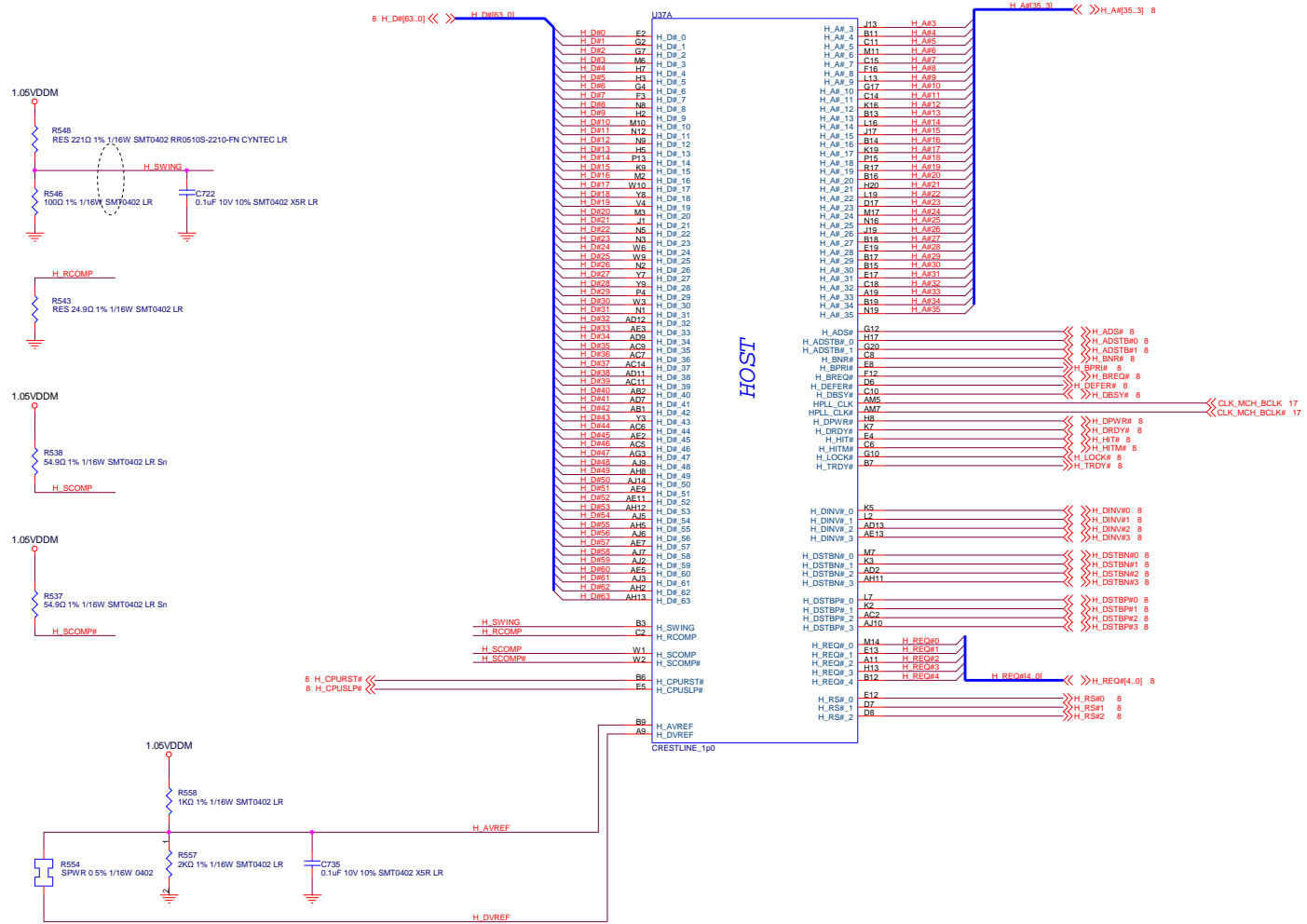
- Q18:** TRANS M-FET-P APM2301AAC-TRL-20V-3A SOT23 3PIN ANPEC LR
- Q19:** NPN PDC144EU SOT-323 PHILIPS LR
- Q17:** TRANS M-FET-N 2N7002 60V 115mA SOT-23 3PIN PSI LR
- Q16:** TRANS M-FET-N 2N7002 60V 115mA SOT-23 3PIN PSI LR
- U10:** LNR-IC Temperature Sensor G784P81U 3.0-5V MSOP-8 8PIN GMT LR
- U55:** LNR-IC Temperature Sensor MAV8657MSA SO 8PIN MAXIM LR
- U63:** COX HR A1250WV-S-03P SMD 3Pin P=125 W=5 ST LR
- U64:** COX HR A1250WV-S-03P SMD 3Pin P=125 W=5 ST LR
- U65:** COX HR A1250WV-S-03P SMD 3Pin P=125 W=5 ST LR
- U66:** COX HR A1250WV-S-03P SMD 3Pin P=125 W=5 ST LR
- U67:** COX HR A1250WV-S-03P SMD 3Pin P=125 W=5 ST LR
- U68:** COX HR A1250WV-S-03P SMD 3Pin P=125 W=5 ST LR
- U69:** COX HR A1250WV-S-03P SMD 3Pin P=125 W=5 ST LR
- U70:** COX HR A1250WV-S-03P SMD 3Pin P=125 W=5 ST LR
- U71:** COX HR A1250WV-S-03P SMD 3Pin P=125 W=5 ST LR
- U72:** COX HR A1250WV-S-03P SMD 3Pin P=125 W=5 ST LR
- U73:** COX HR A1250WV-S-03P SMD 3Pin P=125 W=5 ST LR
- U74:** COX HR A1250WV-S-03P SMD 3Pin P=125 W=5 ST LR
- U75:** COX HR A1250WV-S-03P SMD 3Pin P=125 W=5 ST LR
- U76:** COX HR A1250WV-S-03P SMD 3Pin P=125 W=5 ST LR
- U77:** COX HR A1250WV-S-03P SMD 3Pin P=125 W=5 ST LR
- U78:** COX HR A1250WV-S-03P SMD 3Pin P=125 W=5 ST LR
- U79:** COX HR A1250WV-S-03P SMD 3Pin P=125 W=5 ST LR
- U80:** COX HR A1250WV-S-03P SMD 3Pin P=125 W=5 ST LR
- U81:** COX HR A1250WV-S-03P SMD 3Pin P=125 W=5 ST LR
- U82:** COX HR A1250WV-S-03P SMD 3Pin P=125 W=5 ST LR
- U83:** COX HR A1250WV-S-03P SMD 3Pin P=125 W=5 ST LR
- U84:** COX HR A1250WV-S-03P SMD 3Pin P=125 W=5 ST LR
- U85:** COX HR A1250WV-S-03P SMD 3Pin P=125 W=5 ST LR
- U86:** COX HR A1250WV-S-03P SMD 3Pin P=125 W=5 ST LR
- U87:** COX HR A1250WV-S-03P SMD 3Pin P=125 W=5 ST LR
- U88:** COX HR A1250WV-S-03P SMD 3Pin P=125 W=5 ST LR
- U89:** COX HR A1250WV-S-03P SMD 3Pin P=125 W=5 ST LR
- U90:** COX HR A1250WV-S-03P SMD 3Pin P=125 W=5 ST LR
- U91:** COX HR A1250WV-S-03P SMD 3Pin P=125 W=5 ST LR
- U92:** COX HR A1250WV-S-03P SMD 3Pin P=125 W=5 ST LR
- U93:** COX HR A1250WV-S-03P SMD 3Pin P=125 W=5 ST LR
- U94:** COX HR A1250WV-S-03P SMD 3Pin P=125 W=5 ST LR
- U95:** COX HR A1250WV-S-03P SMD 3Pin P=125 W=5 ST LR
- U96:** COX HR A1250WV-S-03P SMD 3Pin P=125 W=5 ST LR
- U97:** COX HR A1250WV-S-03P SMD 3Pin P=125 W=5 ST LR
- U98:** COX HR A1250WV-S-03P SMD 3Pin P=125 W=5 ST LR
- U99:** COX HR A1250WV-S-03P SMD 3Pin P=125 W=5 ST LR
- U100:** COX HR A1250WV-S-03P SMD 3Pin P=125 W=5 ST LR

Other components include resistors (R123, R133, R171, R173, R95), capacitors (C195, C262, C263, C163), and a diode (D21). The layout also shows various signal and power lines, including 5VDDM, 3VDDM, 3VDDA, and 5VDDM.



NB 965PM : 05-23767-01 (REV. B0)

NB 965GM : 05-23768-01 (REV. B0)



8,9,14,15,17,21,23,50 1.05VDDM 0-1.05VDDM

**FI** First International Computer, Inc.  
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114 TAIPEI, TAIWAN, ROC  
(886-2)8751-8751

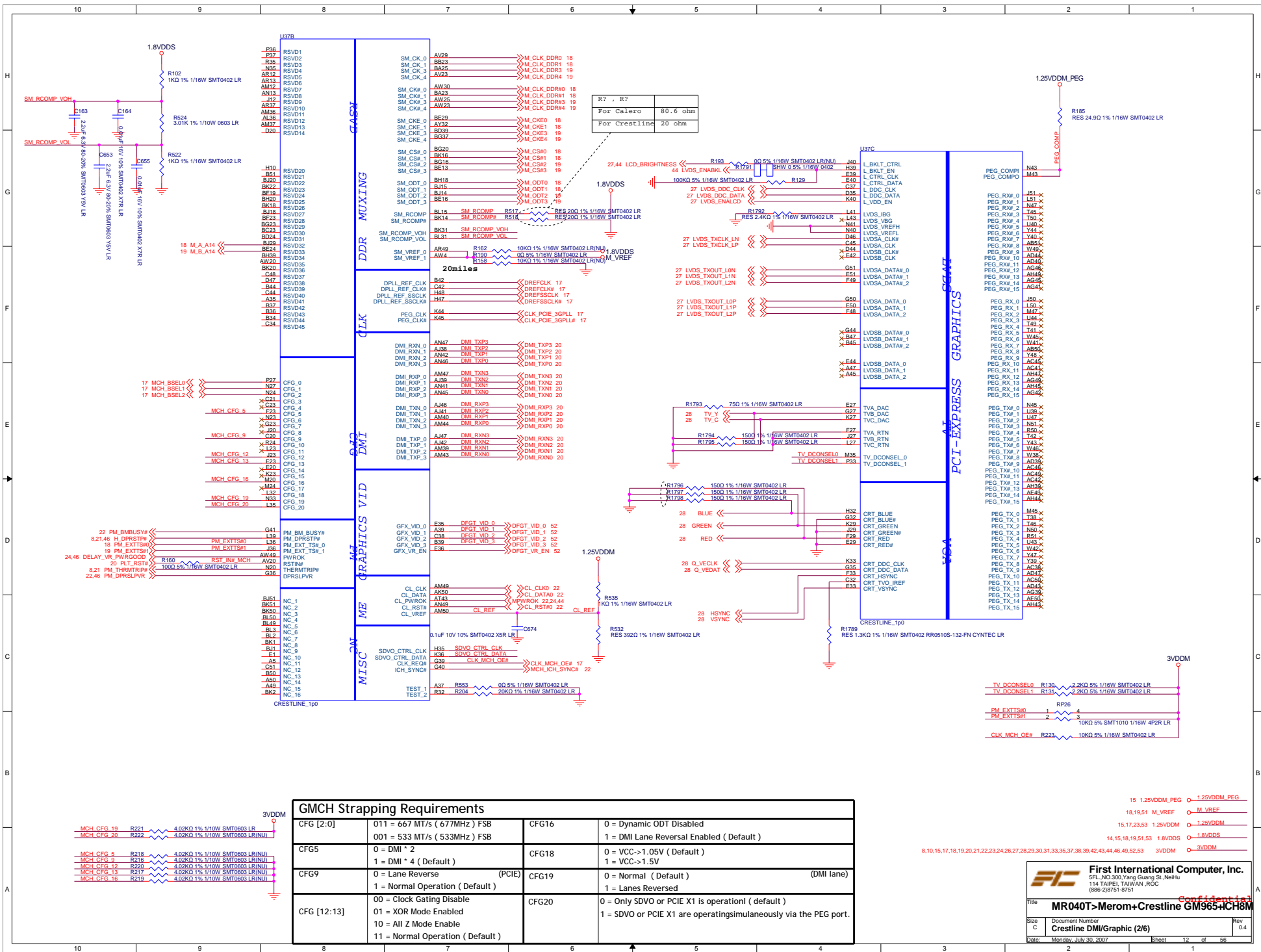
**Confidential**

File: **MR040T>Merom+Crestline GM965+CH8M**

Size: C Document Number: **Crestline Host (1/6)** Rev: 0.4

Date: Monday, July 30, 2007 Sheet: 11 of 56





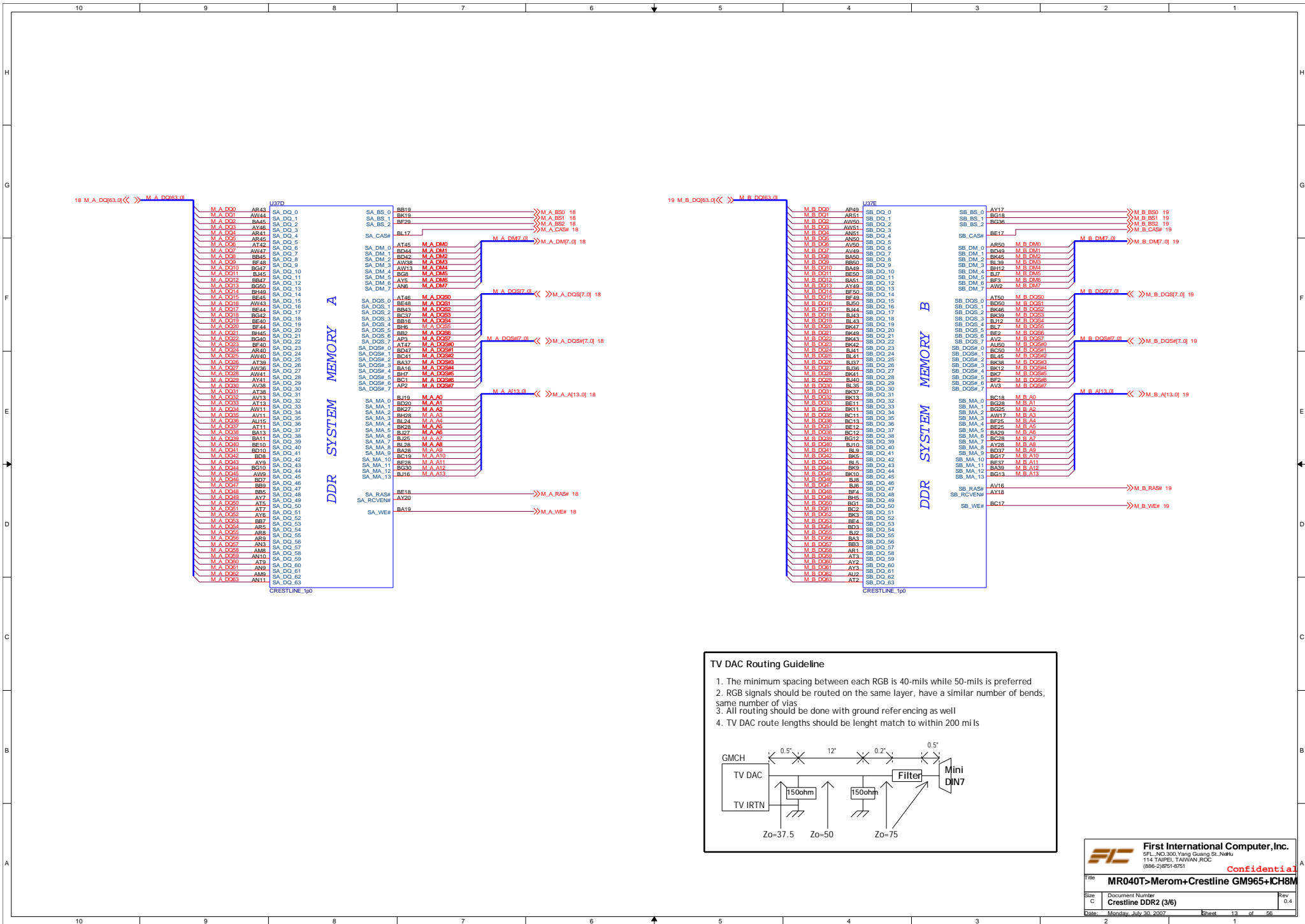
### GMCH Strapping Requirements

CFG [2:0]	011 = 667 MT/s ( 677MHz ) FSB 001 = 533 MT/s ( 533MHz ) FSB	CFG16	0 = Dynamic ODT Disabled 1 = DMI Lane Reversal Enabled ( Default )
CFG5	0 = DMI * 2 1 = DMI * 4 ( Default )	CFG18	0 = VCC->1.05V ( Default ) 1 = VCC->1.5V
CFG9	0 = Lane Reverse (PCIe) 1 = Normal Operation ( Default )	CFG19	0 = Normal ( Default ) 1 = Lanes Reversed ( DMI lane )
CFG [12:13]	00 = Clock Gating Disable 01 = XOR Z Mode Enable 10 = All Z Mode Enable 11 = Normal Operation ( Default )	CFG20	0 = Only SDVO or PCIe X1 is operationl ( default ) 1 = SDVO or PCIe X1 are operatingsimulaneously via the PEG port.

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File: **MR040T+Merom+Crestline GM965+ICH8M**  
Size: **Crestline DMI/Graphic (2/6)**  
Date: **Monday, July 30, 2007** Sheet: **12** of **56**

















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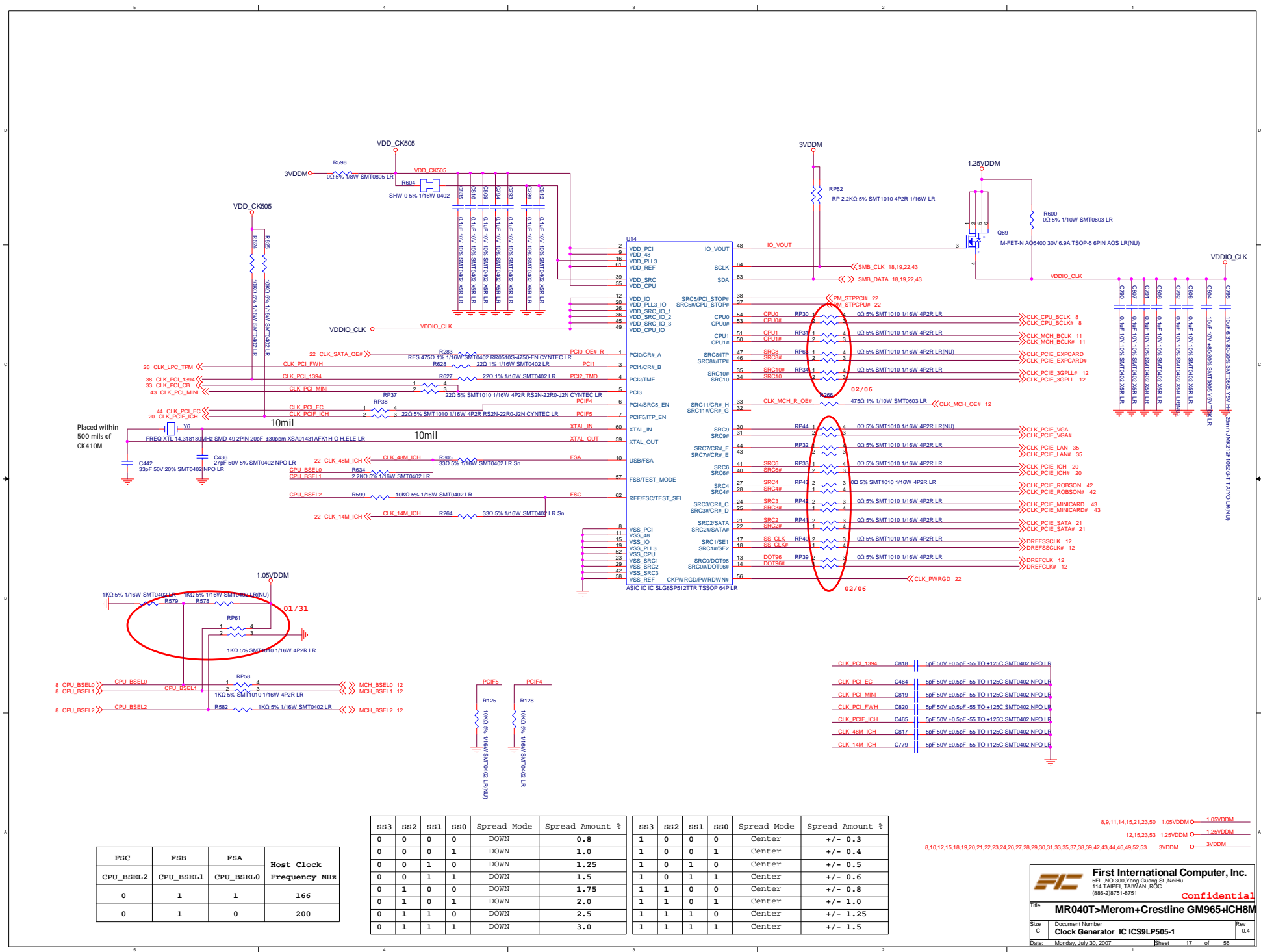


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FSC	FSB	FSA	Host Clock Frequency MHz
CPU_BSEL0	CPU_BSEL1	CPU_BSEL0	166
0	1	1	200

SS3	SS2	SS1	SS0	Spread Mode	Spread Amount %
0	0	0	0	DOWN	0.8
0	0	0	1	DOWN	1.0
0	0	1	0	DOWN	1.25
0	0	1	1	DOWN	1.5
0	1	0	0	DOWN	1.75
0	1	0	1	DOWN	2.0
0	1	1	0	DOWN	2.5
0	1	1	1	DOWN	3.0

SS3	SS2	SS1	SS0	Spread Mode	Spread Amount %
1	0	0	0	Center	+/- 0.3
1	0	0	1	Center	+/- 0.4
1	0	1	0	Center	+/- 0.5
1	0	1	1	Center	+/- 0.6
1	1	0	0	Center	+/- 0.8
1	1	0	1	Center	+/- 1.0
1	1	1	0	Center	+/- 1.25
1	1	1	1	Center	+/- 1.5



First International Computer, Inc.

SFL NO 3301 Yang Guang St. Neihu  
114 TAIPEI, TAIWAN, R.O.C  
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MR040T>Merom+Crestrline GM965+CH8M

Size C Document Number Clock Generator IC CS9LP505-1 Rev 0.4

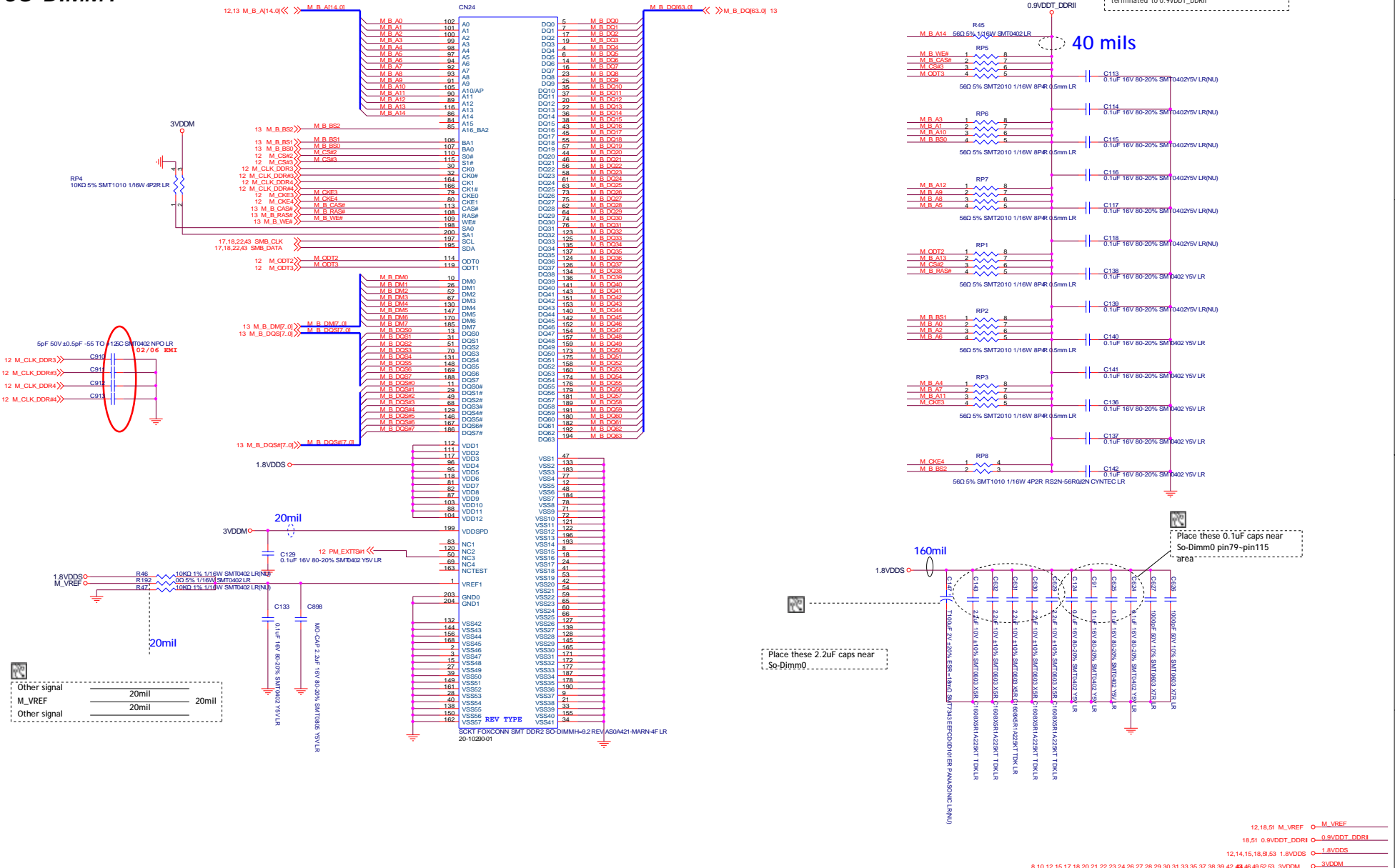
Date Monday, July 30, 2007 Sheet 17 of 56



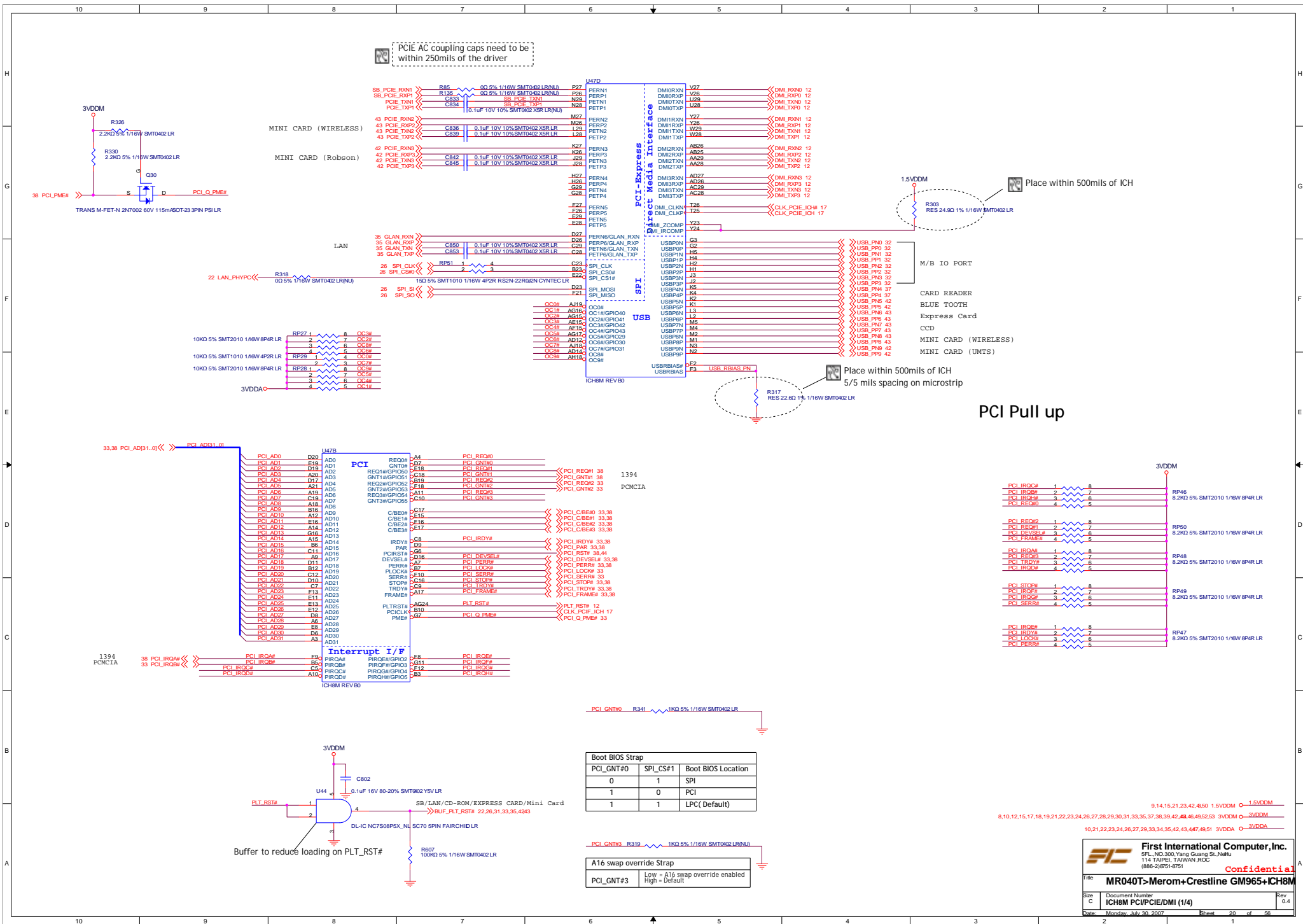
The image displays a detailed PCB layout for an SO-DIMM0 module. The layout includes various components such as resistors (R56, R57, R58, R59, R60, R61, R62, R63, R64, R65, R66, R67, R68, R69, R70, R71, R72, R73, R74, R75, R76, R77, R78, R79, R80, R81, R82, R83, R84, R85, R86, R87, R88, R89, R90, R91, R92, R93, R94, R95, R96, R97, R98, R99, R100), capacitors (C90, C91, C92, C93, C94, C95, C96, C97, C98, C99, C100, C101, C102, C103, C104, C105, C106, C107, C108, C109, C110, C111, C112, C113, C114, C115, C116, C117, C118, C119, C120, C121, C122, C123, C124, C125, C126, C127, C128, C129, C130, C131, C132, C133, C134, C135, C136, C137, C138, C139, C140, C141, C142, C143, C144, C145, C146, C147, C148, C149, C150, C151, C152, C153, C154, C155, C156, C157, C158, C159, C160, C161, C162, C163, C164, C165, C166, C167, C168, C169, C170, C171, C172, C173, C174, C175, C176, C177, C178, C179, C180, C181, C182, C183, C184, C185, C186, C187, C188, C189, C190, C191, C192, C193, C194, C195, C196, C197, C198, C199, C200, C201, C202, C203, C204, C205, C206, C207, C208, C209, C210, C211, C212, C213, C214, C215, C216, C217, C218, C219, C220, C221, C222, C223, C224, C225, C226, C227, C228, C229, C230, C231, C232, C233, C234, C235, C236, C237, C238, C239, C240, C241, C242, C243, C244, C245, C246, C247, C248, C249, C250, C251, C252, C253, C254, C255, C256, C257, C258, C259, C260, C261, C262, C263, C264, C265, C266, C267, C268, C269, C270, C271, C272, C273, C274, C275, C276, C277, C278, C279, C280, C281, C282, C283, C284, C285, C286, C287, C288, C289, C290, C291, C292, C293, C294, C295, C296, C297, C298, C299, C300, C301, C302, C303, C304, C305, C306, C307, C308, C309, C310, C311, C312, C313, C314, C315, C316, C317, C318, C319, C320, C321, C322, C323, C324, C325, C326, C327, C328, C329, C330, C331, C332, C333, C334, C335, C336, C337, C338, C339, C340, C341, C342, C343, C344, C345, C346, C347, C348, C349, C350, C351, C352, C353, C354, C355, C356, C357, C358, C359, C360, C361, C362, C363, C364, C365, C366, C367, C368, C369, C370, C371, C372, C373, C374, C375, C376, C377, C378, C379, C380, C381, C382, C383, C384, C385, C386, C387, C388, C389, C390, C391, C392, C393, C394, C395, C396, C397, C398, C399, C400, C401, C402, C403, C404, C405, C406, C407, C408, C409, C410, C411, C412, C413, C414, C415, C416, C417, C418, C419, C420, C421, C422, C423, C424, C425, C426, C427, C428, C429, C430, C431, C432, C433, C434, C435, C436, C437, C438, C439, C440, C441, C442, C443, C444, C445, C446, C447, C448, C449, C450, C451, C452, C453, C454, C455, C456, C457, C458, C459, C460, C461, C462, C463, C464, C465, C466, C467, C468, C469, C470, C471, C472, C473, C474, C475, C476, C477, C478, C479, C480, C481, C482, C483, C484, C485, C486, C487, C488, C489, C490, C491, C492, C493, C494, C495, C496, C497, C498, C499, C500, C501, C502, C503, C504, C505, C506, C507, C508, C509, C510, C511, C512, C513, C514, C515, C516, C517, C518, C519, C520, C521, C522, C523, C524, C525, C526, C527, C528, C529, C530, C531, C532, C533, C534, C535, C536, C537, C538, C539, C540, C541, C542, C543, C544, C545, C546, C547, C548, C549, C550, C551, C552, C553, C554, C555, C556, C557, C558, C559, C560, C561, C562, C563, C564, C565, C566, C567, C568, C569, C570, C571, C572, C573, C574, C575, C576, C577, C578, C579, C580, C581, C582, C583, C584, C585, C586, C587, C588, C589, C590, C591, C592, C593, C594, C595, C596, C597, C598, C599, C600, C601, C602, C603, C604, C605, C606, C607, C608, C609, C610, C611, C612, C613, C614, C615, C616, C617, C618, C619, C620, C621, C622, C623, C624, C625, C626, C627, C628, C629, C630, C631, C632, C633, C634, C635, C636, C637, C638, C639, C640, C641, C642, C643, C644, C645, C646, C647, C648, C649, C650, C651, C652, C653, C654, C655, C656, C657, C658, C659, C660, C661, C662, C663, C664, C665, C666, C667, C668, C669, C670, C671, C672, C673, C674, C675, C676, C677, C678, C679, C680, C681, C682, C683, C684, C685, C686, C687, C688, C689, C690, C691, C692, C693, C694, C695, C696, C697, C698, C699, C700, C701, C702, C703, C704, C705, C706, C707, C708, C709, C710, C711, C712, C713, C714, C715, C716, C717, C718, C719, C720, C721, C722, C723, C724, C725, C726, C727, C728, C729, C730, C731, C732, C733, C734, C735, C736, C737, C738, C739, C740, C741, C742, C743, C744, C745, C746, C747, C748, C749, C750, C751, C752, C753, C754, C755, C756, C757, C758, C759, C760, C761, C762, C763, C764, C765, C766, C767, C768, C769, C770, C771, C772, C773, C774, C775, C776, C777, C778, C779, C780, C781, C782, C783, C784, C785, C786, C787, C788, C789, C790, C791, C792, C793, C794, C795, C796, C797, C798, C799, C800, C801, C802, C803, C804, C805, C806, C807, C808, C809, C810, C811, C812, C813, C814, C815, C816, C817, C818, C819, C820, C821, C822, C823, C824, C825, C826, C827, C828, C829, C830, C831, C832, C833, C834, C835, C836, C837, C838, C839, C840, C841, C842, C843, C844, C845, C846, C847, C848, C849, C850, C851, C852, C853, C854, C855, C856, C857, C858, C859, C860, C861, C862, C863, C8



# SO-DIMM1

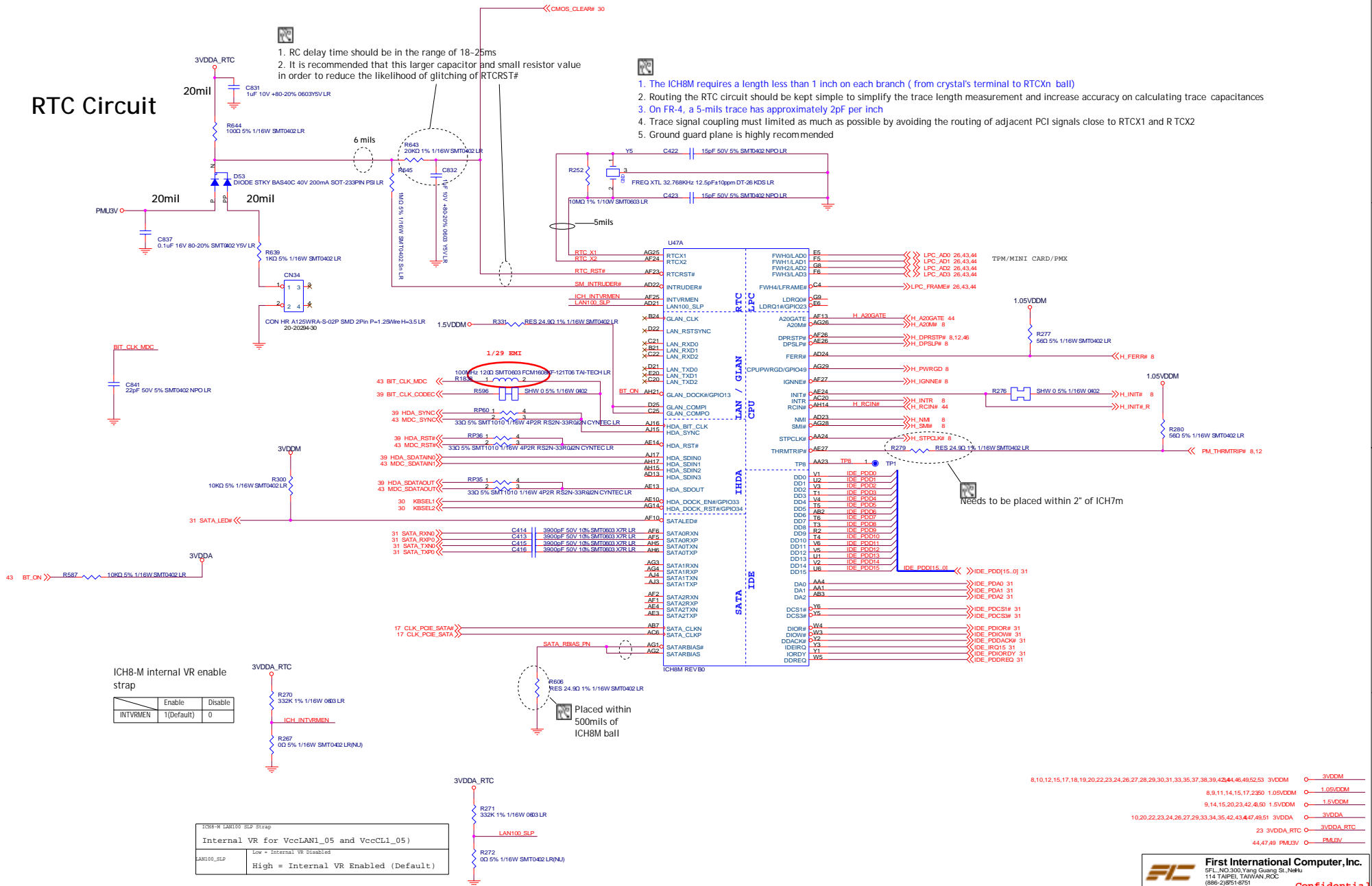








## RTC Circuit








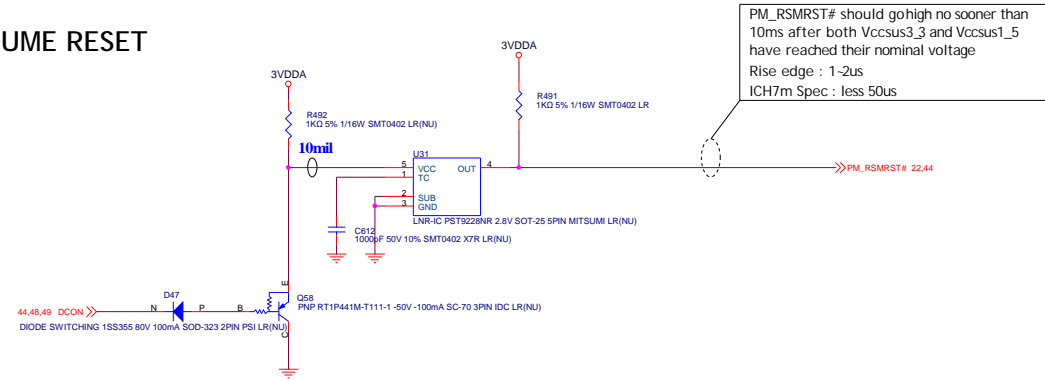




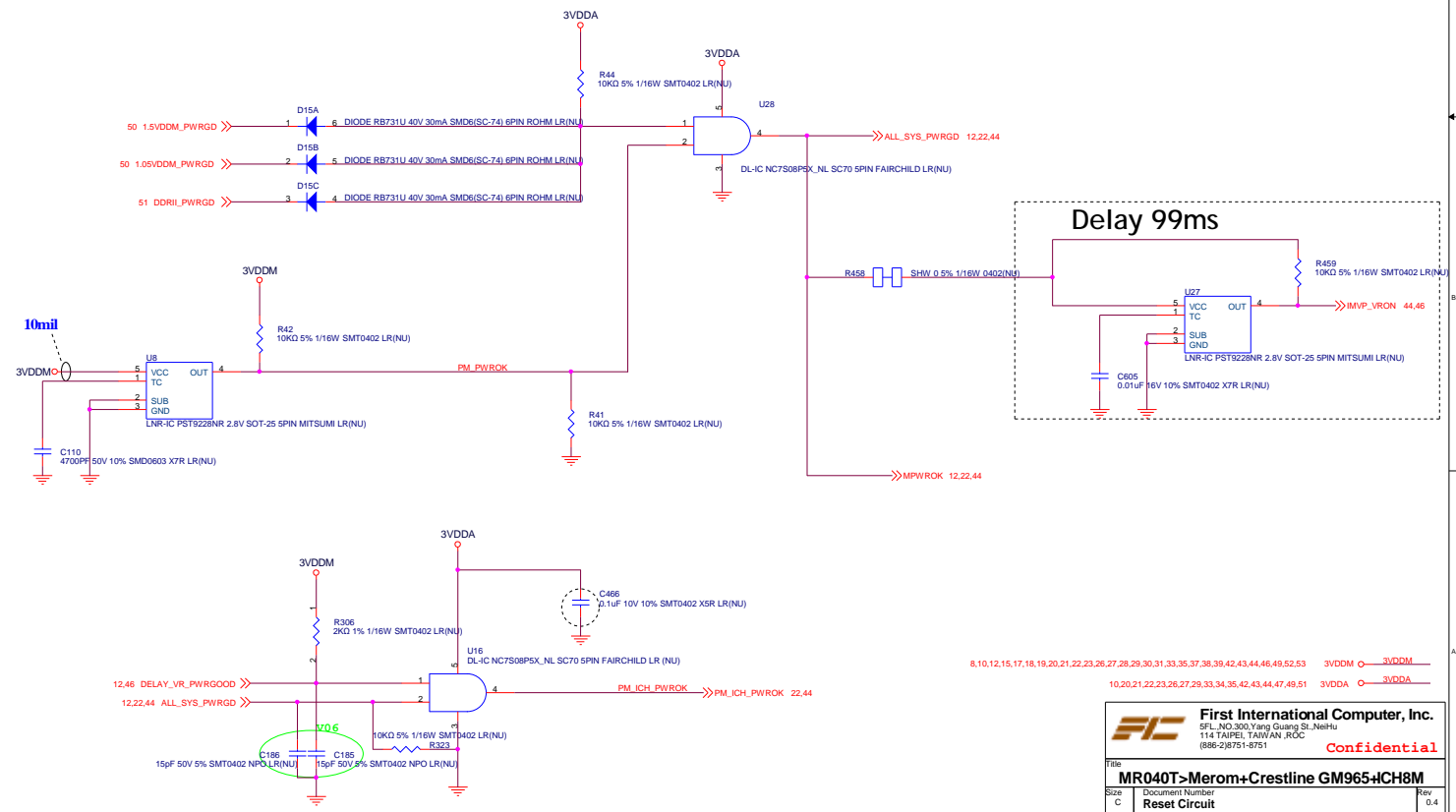
 <b>First International Computer, Inc.</b> 5FL NO.300,Yang Gung St.-Nehhu 114 TAIPEI, TAIWAN ,ROC (086-2)8751-3751		<b>Confidential</b>
Title	<b>MR0407+Merom+Crestline GM965+CH8M</b>	
Size	Document Number <b>ICH8M Power/GND (4/4)</b>	Rev <b>0.4</b>
Date	Monday, July 30, 2007	Sheet 23 of 56



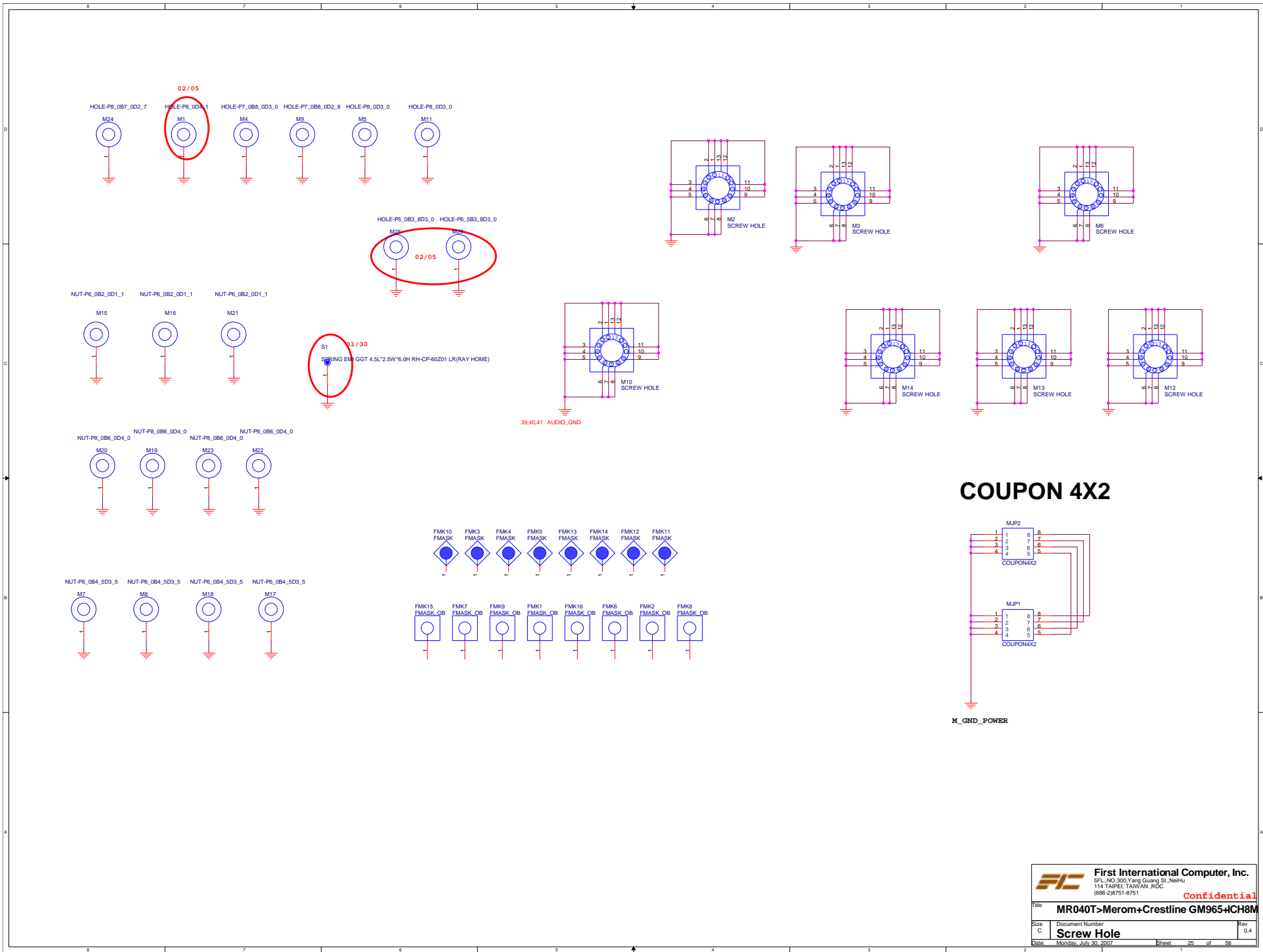
RESUME RESET



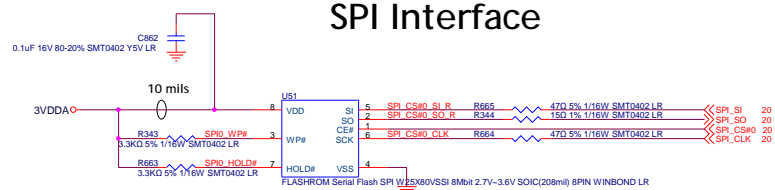
NAPA Platform Power Good Circuit





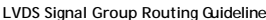




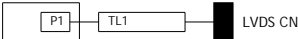


## SPI Interface





GMCH



Topology	Differential Pair Point-to-Point
Reference Plane	Ground
Differential Mode Impedance	100 +/- 20%
Nominal Trace Width	4 mils
Nominal Pair Spacing (Edge to edge)	7 mils
Minimum Pair-to-Pair Spacing	20 mils
Minimum Serpentine Spacing	20 mils
Minimum Spacing to Other LVDS	20 mils
Minimum Isolation Spacing to no n-LVDS	20 mils
Maximim Via Count	2 (per line)
Package Length Range - P1	750 mils +/- 250 mils
Total MB Length - TL1	Max = 10"
Length Matching with Pair	Matching to within +/- 20mils
Clock to Data Length Matching (Total Length)	Matching Data to Clock within +/- 20mils
Clock A to Clock B Length Matching	Match Clock A to B within +/- 20mils
Breakout Exceptions (Reduce geometries for GCMC break-out region)	4/4 mils spacing allowed and 10 mils Pair-to-Pair spacing allowed Max. breakout length is 500 mils

\*\*\*Cable Length must be less than 16"

## LCD brightness control from PMX







		CNR	
44	X0	1	
44	X1	2	
44	X2	3	
44	Y0	4	
44	Y1	5	
44	Y2	6	
44	Y3	7	
44	X3	8	
44	Y4	10	
44	Y5	11	TRAN
44	Y6	12	
44	X5	14	
44	X7	16	
44	X8	17	
44	X9	18	
44	X10	19	
44	X11	21	
44	X12	22	
44	X13	23	
44	X15	24	

CON ACES SMT-FPC 24PIN Pu-0.10 9H±2.8mm 2R 85201-2402 LRG  
20-243111-11

The diagram illustrates a complex PCB layout for a 402G LR device. Key components and their connections include:

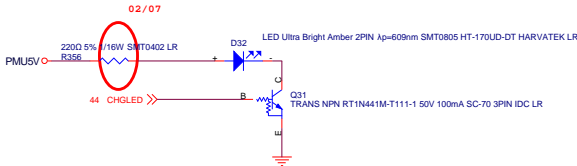
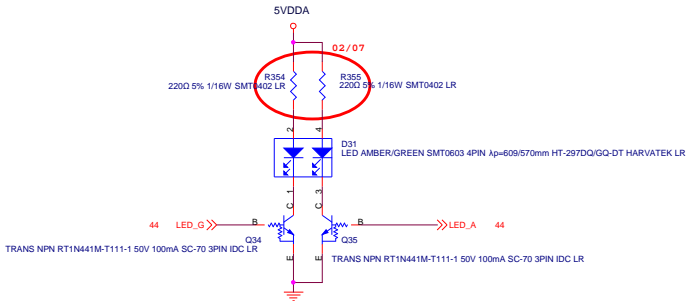
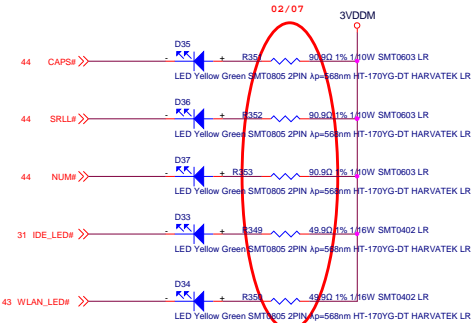
- Power Management:** VDDMO and VDDAT supply rails are shown with decoupling capacitors (C384, C385, C390) and inductors (L42, L43, L48). A 5V regulator (U3) is also present.
- Transistors:** Q76 (MOSFET) and Q77 (BJT) are used for signal processing or switching.
- Resistors:** Various resistors (R67, R348, R345, R346, R347) are placed for biasing and signal conditioning.
- Capacitors:** Multiple capacitors (C384, C385, C390, C319, C320) are used for decoupling and timing.
- Inductors:** Inductors (L42, L43, L48) are used for impedance matching and filtering.
- Switches:** SW1, SW2, SW3, and SW4 are mechanical switches used for testing or configuration.
- Connectors:** CON1 (12-pin) and CON2 (4-pin) are used for external connections.
- Labels:** The layout includes labels for "RIGHT" and "LEFT" sides, indicating the device's orientation.

[illegible]

Title			
MR040T>Merom+Crestline GM965+ICH8M			
Size	Document Number	Rev	
C	<INT K/B /GP/SW CNN>	0.4	
Date:	Monday, July 30, 2007	Sheet	29 of 56



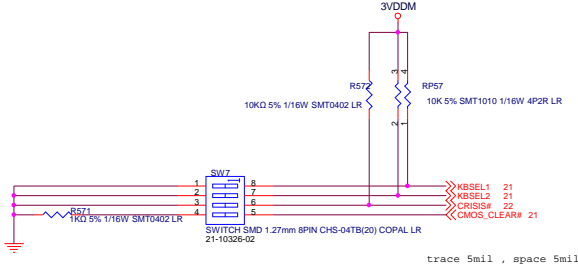
LED indicator control logic



D?? D32 D33 D34 D35 D36 D37



DIP SWITCH



KBSEL2	KBSEL1	
ON	ON	UK Keyboard
OFF	OFF	Reserved
OFF	OFF	JP Keyboard
OFF	OFF	US Keyboard

MB_ID0	ON	Reserved
	OFF	Reserved
LOGSEL	ON	Reserved
	OFF	Reserved
PASS0	ON	Override
	OFF	Available
DVDSEL	ON	CD-ROM
	OFF	DVD
CMOS_CLEAR	ON	Reset RTC
	OFF	NONE

8,10,12,15,17,18,19,20,21,22,23,24,26,27,28,29,31,33,35,37,38,39,42,43,44,46,49,52,53 3VDDM  
23,32,34,43,46,49,50,51,52,53 5VDDA  
44,49 PMUSV

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File: **MR040T>Merom+Crestline GM965+CH8M**

Size: C Document Number: **<DIP SW/LED>** Rev: 0.1

Date: Monday, July 30, 2007 Sheet: 30 of 56



# NOTE

SATA differential stripline 20:5:6:5:20  
SATA differential microstripline 20:6:6:6:20  
請包GROUND



## SATA Layout Note:

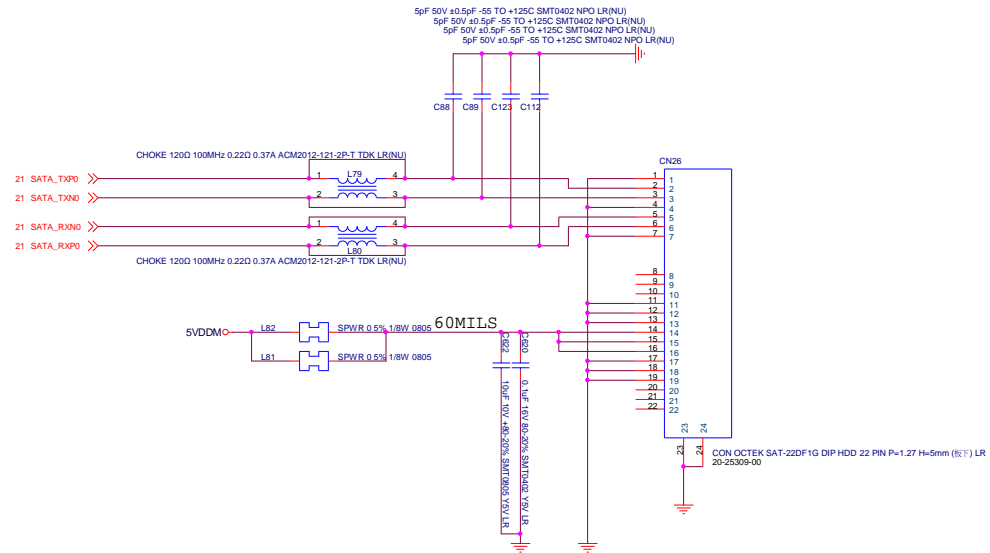
MS or SL:

6mils 6mils 6mils 6mils  
20mils 6mils 20mils 6mils 20mils

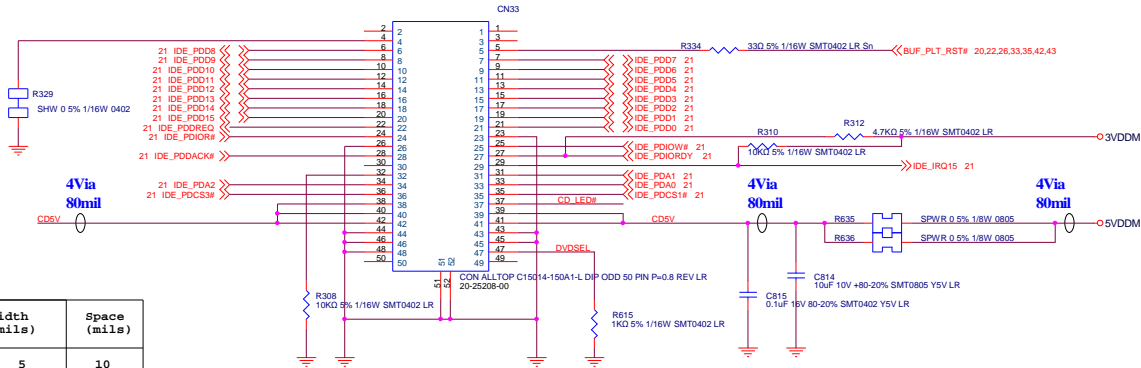
TX

RX

- \* Zdiff = 100 Ohm +/- 10%. TX & RX should refer GND.No via & stubs.The Best layer is Top.
- \* TX/RX trace length < 2 inches.
- \* TX+/- need matching trace ±10 mils length.
- \* RX+/- need matching trace ±10 mils length.
- \* SATA Pair to Pair Trace matching trace ±10 mils length.



## CD-ROM CNN



### IDE Signals

Signals	MAX Length (inch)	Width (mils)	Space (mils)
IDE_PDD[15:0]	8	5	10
IDE_SDD[15:0]	8	5	10
IDE_PDA0-2	8	5	10
IDE_SDA0-2	8	5	10
IDE_PDCS 10-30#	8	5	10
IDE_PDDREQ	8	5	10
IDE_SDDREQ	8	5	10
IDE_PDIOW#	8	5	10
IDE_PATADET	8	5	10
IDE_SATADET	8	5	10
IDE_PDDACK#	8	5	10
IDE_SDDACK#	8	5	10

8,10,12,15,17,18,19,20,21,22,23,24,26,27,28,29,30,33,35,37,38,39,42,43,44,46,49,52,53 3VDDM  
10,23,28,29,40,41,49 5VDDM

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File: **MR040T>Merom+Crestline GM965+CH8M**

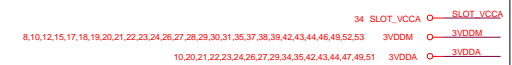
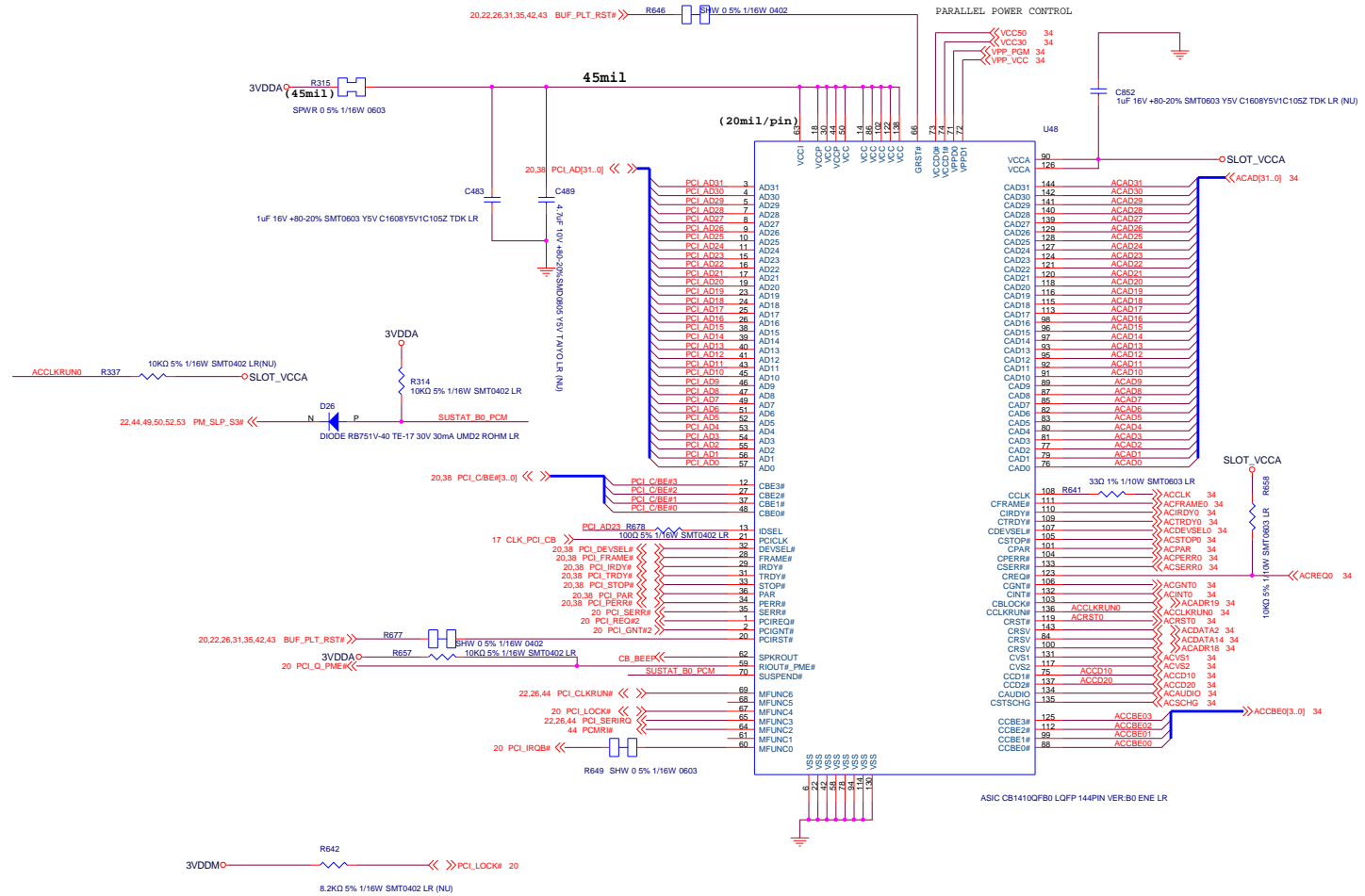
Size: C Document Number: **<IDE connector>** Rev: 0.4

Date: Monday, July 30, 2007 Sheet: 31 of 56

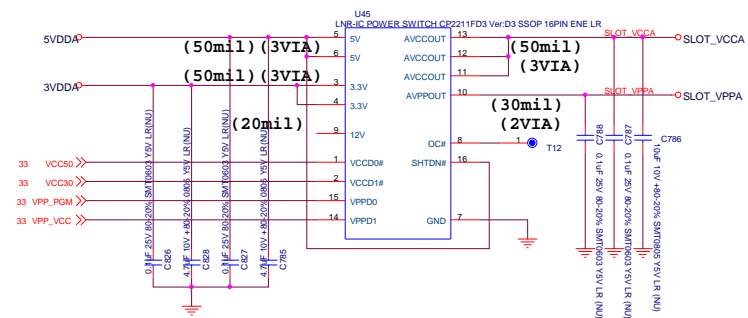













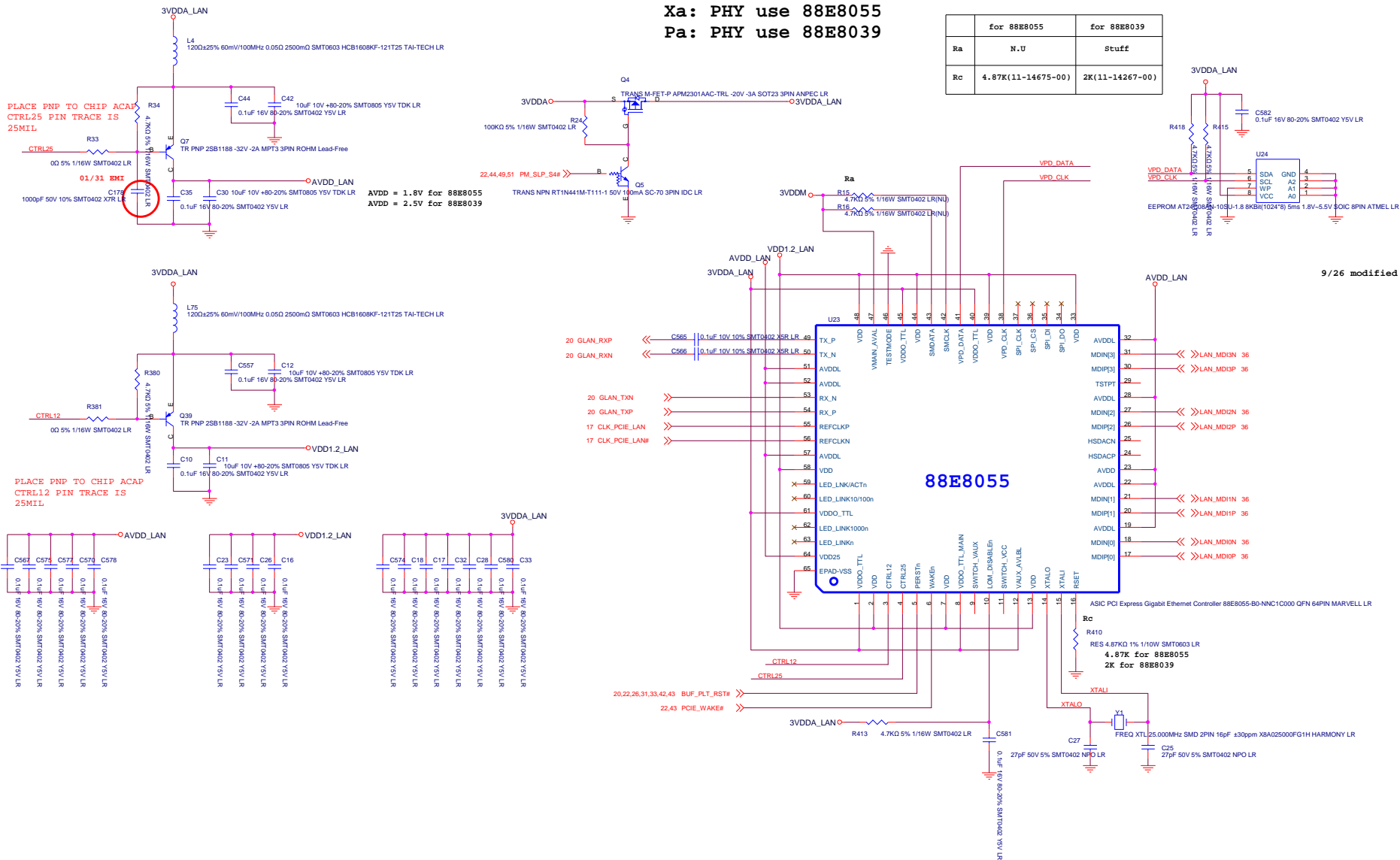
 <b>First International Computer, Inc.</b> 5FL NO.303,Yang Guang St.,Neihu 114 TAIPEI, TAIWAN, R.O.C (886-2)8751-8751		<b>Confidential</b>	
Title <b>MR040T&gt;Merom+Crestline GM965+ICH8M</b>			
Size C	Document Number	Rev 0.4	
> CardBus Power/CNN >			
Date:	Monday, July 30, 2007	Sheet	34 of 56



Xa: PHY use 88E8055

Pa: PHY use 88E8039

	for 88E8055	for 88E8039
Ra	N.U	Stuff
Rc	4.87K(11-14675-00)	2K(11-14267-00)



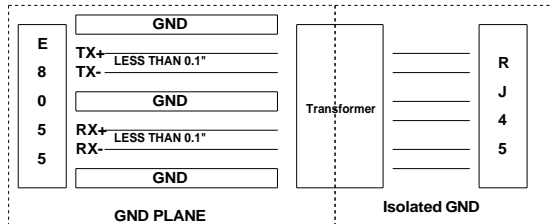
#### Layout Guide

1. The Lan Chip should be placed as close as possible to the transfer.
2. The resistor connected to RSET pin should be placed near to the Lan Chip, and away from signal traces(ex:MDIO/-) and clock signals as far as possible.
3. The transfer should be placed as close as possible to the RJ45 connector.
4. The crystal should be placed far away from I/O ports and high frequency signal.
5. The termination resistors and capacitors should be placed closely to the Lan Chip.
6. The decoupling capacitors should be placed as close as possible to the power pins, such that the distance from IC power pin to the capacitor is within 200mils.
7. Traces routed from the Lan Chip to the transfer, and to the RJ45 connector should be as short as possible.
8. The 10-12cm maximum length between Lan Chip and transfer is achievable only when there's no interferences around.
9. All 4 pairs of the differential resistor(49.9k) must close to Lan Chip, and make them 4 pairs as name as distant.
10. PLACE GND PLANE AS LARGE AS POSSIBLE
11. If power pins are next to each other and there is not much room to accommodate multiple capacitors, then the power pins can share the same capacitors.
12. It's important to separate digital signals from analog signals. If it is unavoidable to cross digital signals with analog power do it at 90 degree angle.
13. The digital power plane should be separated from analog areas.
14. All analog decoupling capacitors should be placed as close to the IC as possible and the traces should be short.
15. The Lan Chip pin 1 facing the transformer, then you can make the signal shorter.

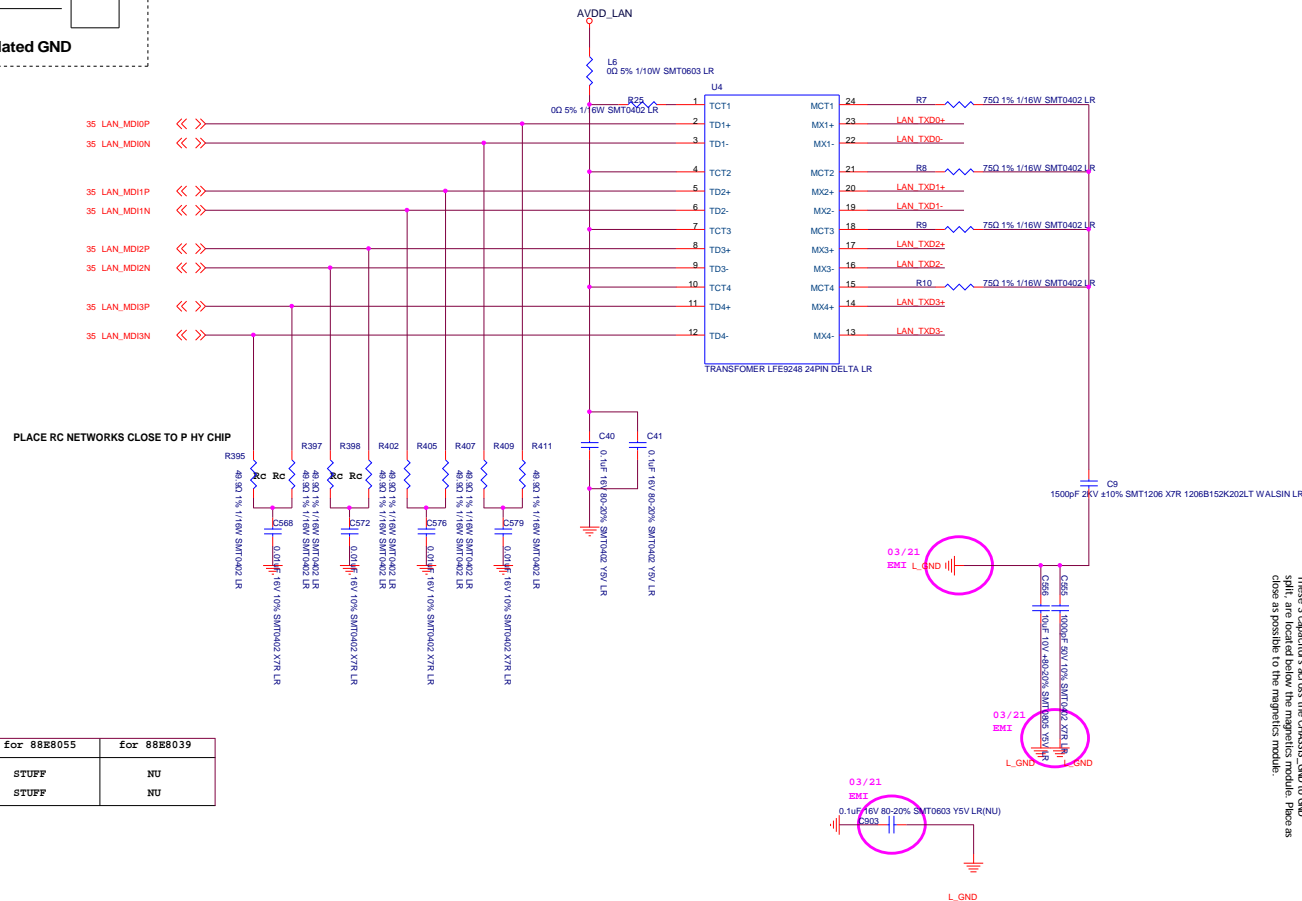
<b>First International Computer, Inc.</b> 5FL IND 300 Yang Guang St., Neihu 114 TAIPEI, TAIWAN, R.O.C (886-2)8751-6751		
<b>Confidential</b>		
File: <b>MR040T&gt;Merom+Crestline GM965+ICH8M</b>		
Size: C	Document Number: <b>PCIE GIGA LAN PHY 88E8055</b>	Rev: 0.4
Date: Monday, July 30, 2007	Ed: 1	35 of 56



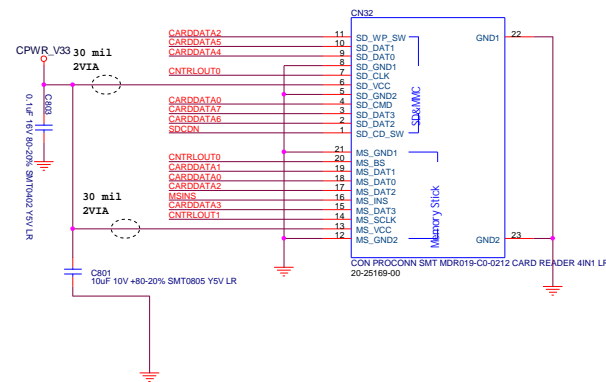
TX 100 ohm ---> trace 4 mil , space 10 mil  
 RX 50 mil space from other signals  
 Total Trace Length no more than 4.8"  
 2 Differential pairs must have the same length



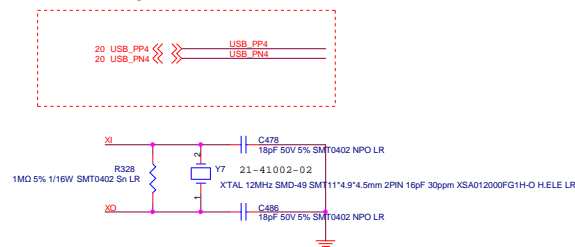
Xa: Transformer use LFE9248(12-01904-01)  
 Pa: Transformer use LFE8450(12-01905-01)







## INTERFACE

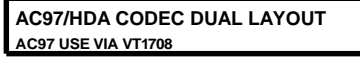


8.10.12.15.17.18.19.20.21.22.23.24.26.27.28.29.30.31.33.35.38.39.42.43.44.46.49.52.53 3VDDM  3VDDM















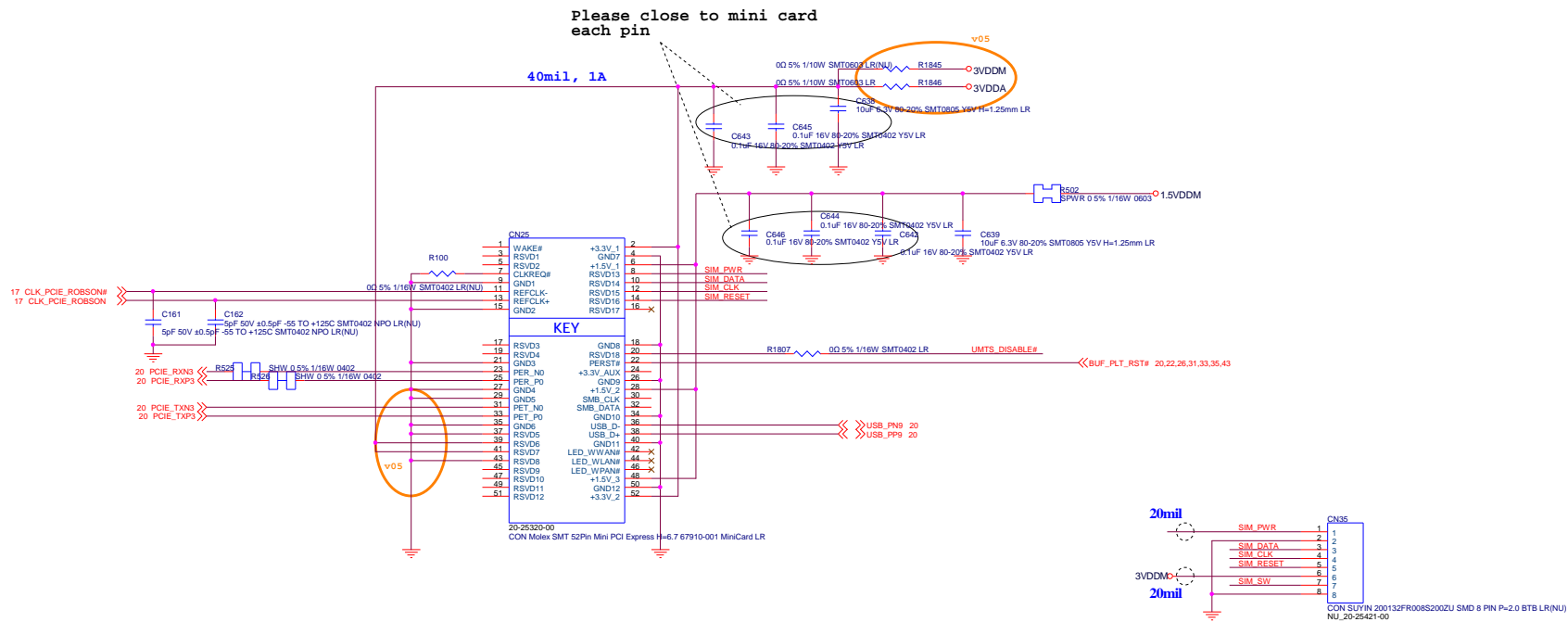
The schematic shows the internal circuitry of the MIC1IN pin. It includes a pull-up resistor RP4 (4.7KΩ) connected to VDD. The input signal from the MIC1IN\_ID pin passes through a series of capacitors (C406, C407) and inductors (L50, L51) before reaching the internal logic. A decoupling capacitor C364 (1000pF) is connected to ground at the input stage. The output of the internal logic is connected to the MIC2IN pin through a series of capacitors (C370, C364) and inductors (L39, L37). The output also has a pull-down resistor RPD4 (4.7KΩ) connected to GND.

The schematic diagram illustrates the microphone input circuitry for the ADAS1000 evaluation board. It features two microphone inputs, IN\_MIC\_L and IN\_MIC\_R, which are connected to a diode switcher (D57) and then to two operational amplifiers (U50A and U50B). The inputs are biased through resistors R674 and R675, and R661 and R662 respectively. The op-amp outputs are connected to INMIC\_L and INMIC\_R. The schematic includes component values such as 4.7K, 10K, 100K, 1M, and 10uF, and part numbers like SMT0603, SMT0402, and SMD 402.

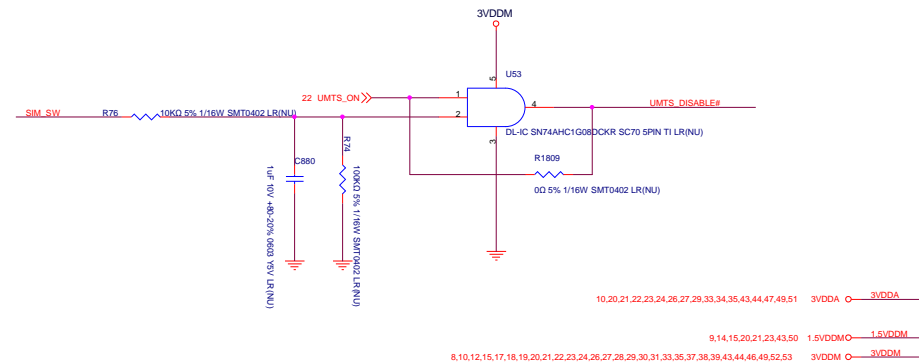
[illegible]



# PCIE Mini Card for Robson/UMTS



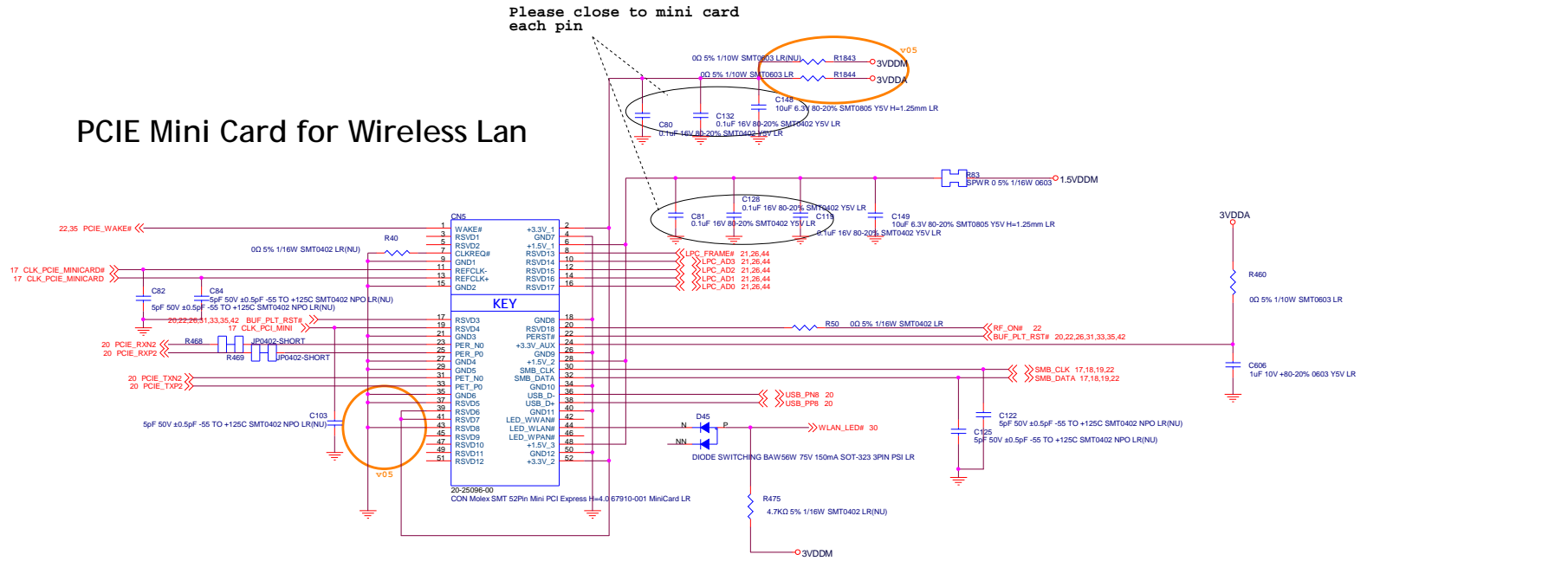
## SIM Card Switch



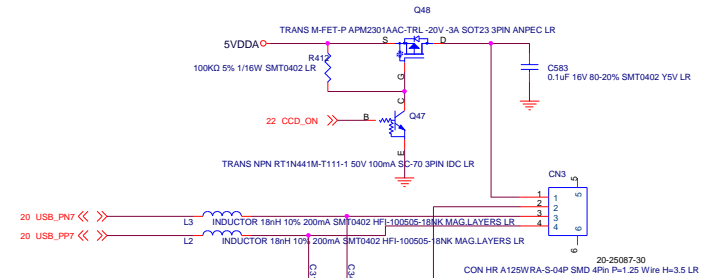
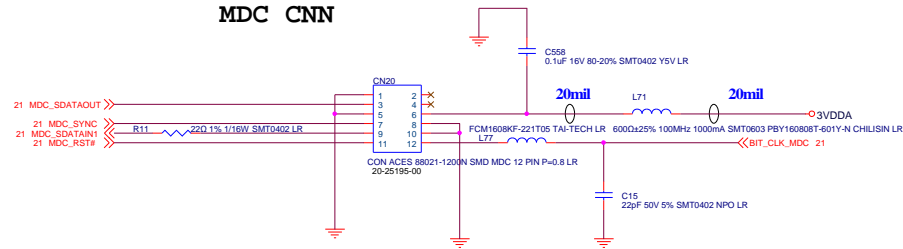
<b>First International Computer, Inc.</b> 5FL AND 300 Yang Guang St., Neihu 114 TAIPEI, TAIWAN, R.O.C. (886-2)8751-6751			
Confidential			
Title <b>MR040T&gt;Merom+Crestline GM965+CH8M</b>			
Size	Document Number	PCIE Mini /UMTS	
Date	Monday, July 30, 2007	Rev	0.4
Sheet		52	of 56



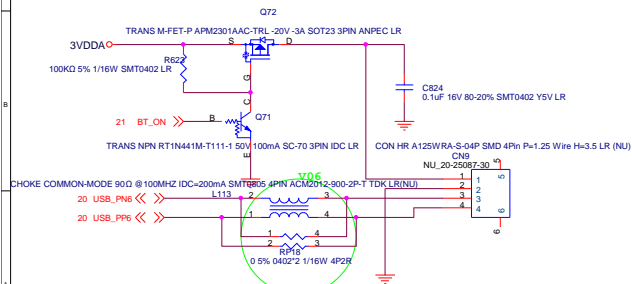
# PCIE Mini Card for Wireless Lan



## MDC CNN



## CCD Module CN



## USI Bluetooth USB Module CN

Reserve

8,10,12,15,17,18,19,20,21,22,23,24,26,27,28,29,30,31,33,35,37,38,39,42,44,46,49,52,53

9,14,15,20,21,23,42,50 1.5VDDM ○ 1.5VDDM

3VDDM ○ 3VDDM

10,20,21,22,23,24,26,27,29,33,34,35,42,44,47,49,51

3VDDA ○ 3VDDA

23,30,32,34,46,49,50,51,52,53

5VDDA ○ 5VDDA

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Title <b>MR040T&gt;Merom+Crestline GM965+CH8M</b>		
Size <b>C</b>	Document Number <b>PCIE Mini /MDC/Bluetooth</b>	Rev <b>0.4</b>
Date: <b>Monday, July 30, 2007</b>	Sheet <b>43 of 56</b>	



# SYSTEM POWER OVP

## PMX

### BATTERY VOLTAGE SENSE

Close to PMX

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(886-2)871-8751

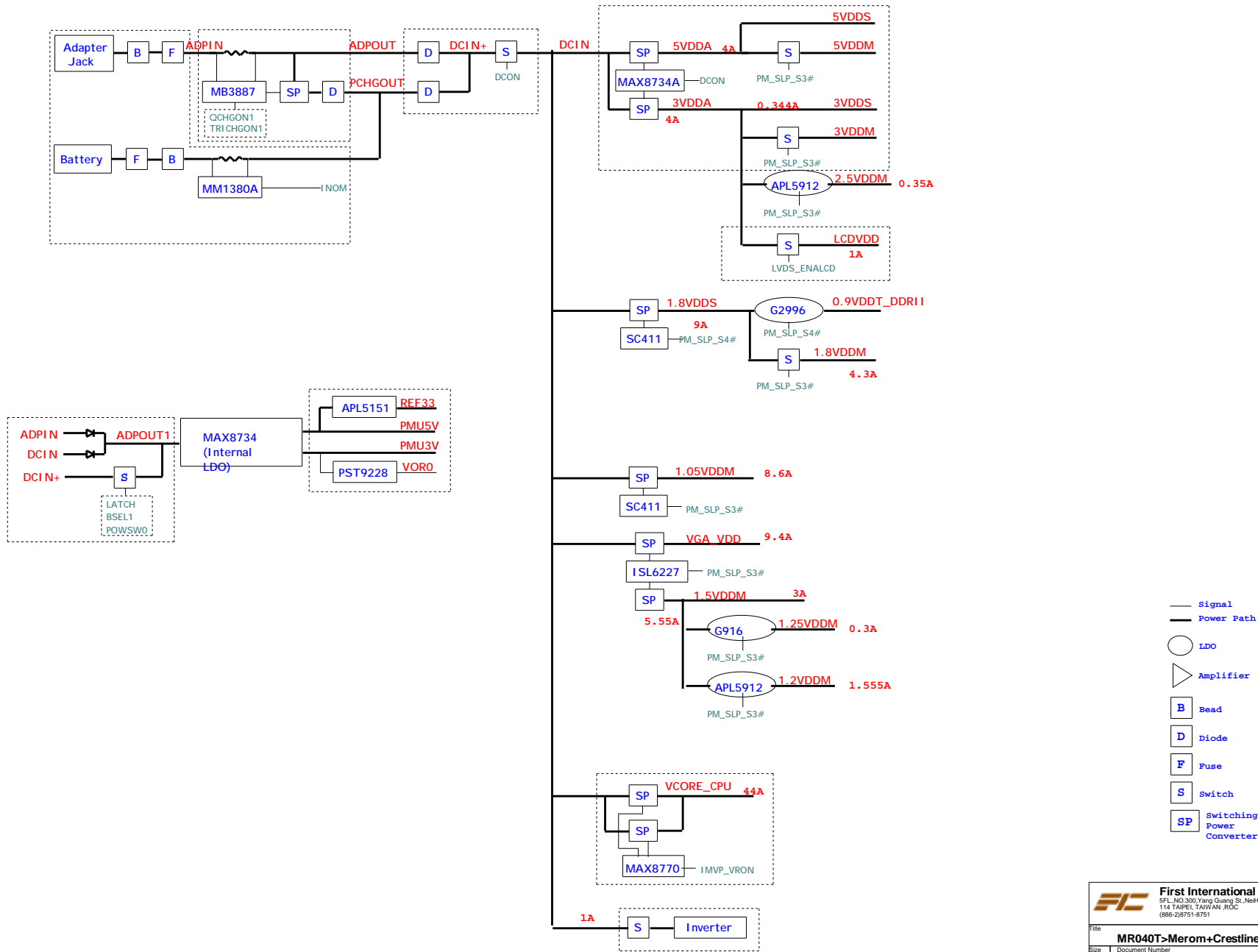
Confidential

MR040T>Merom+CreStine GM965+ICH8M

Doc: PMX  
Customer: PMX  
Date: Monday, July 30, 2007  
Sheet: 44 of 66



# PR341 Power Block

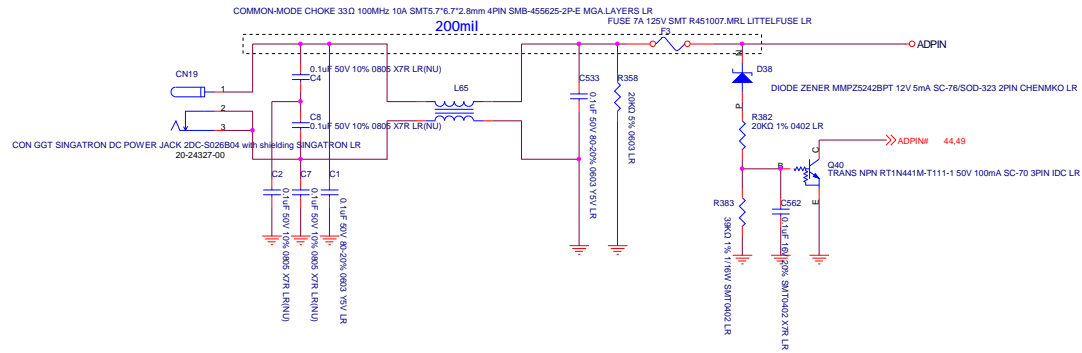




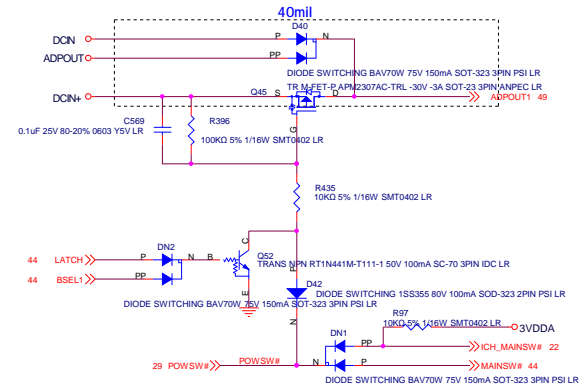




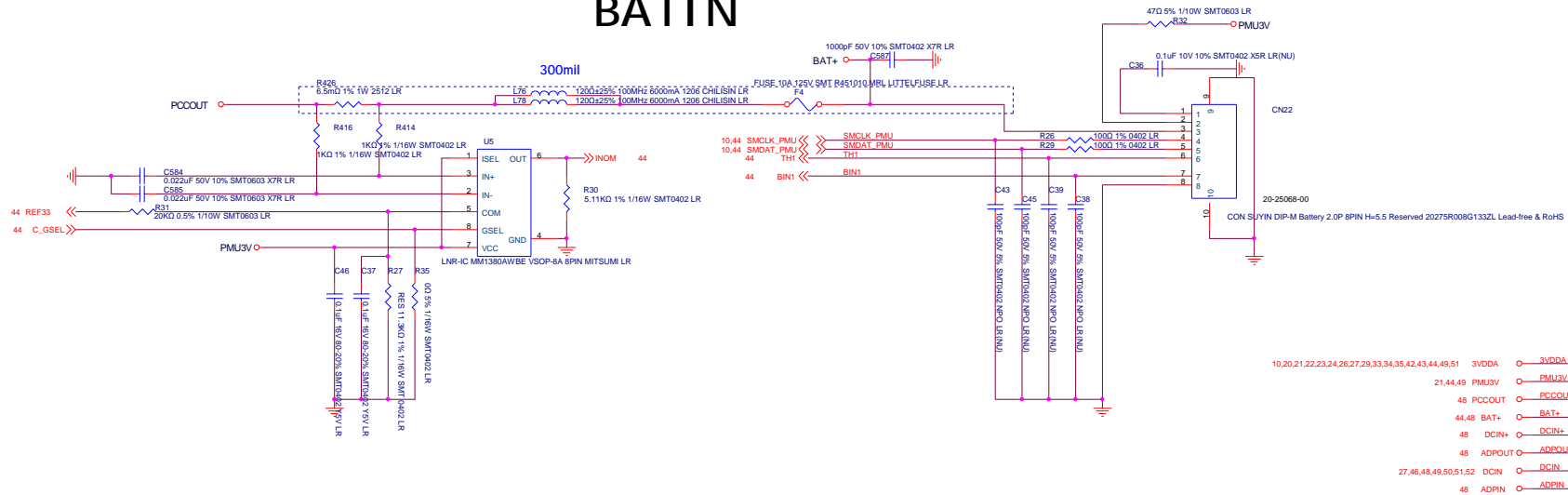
# ADPIN



# ADPOUT1



# BATIN

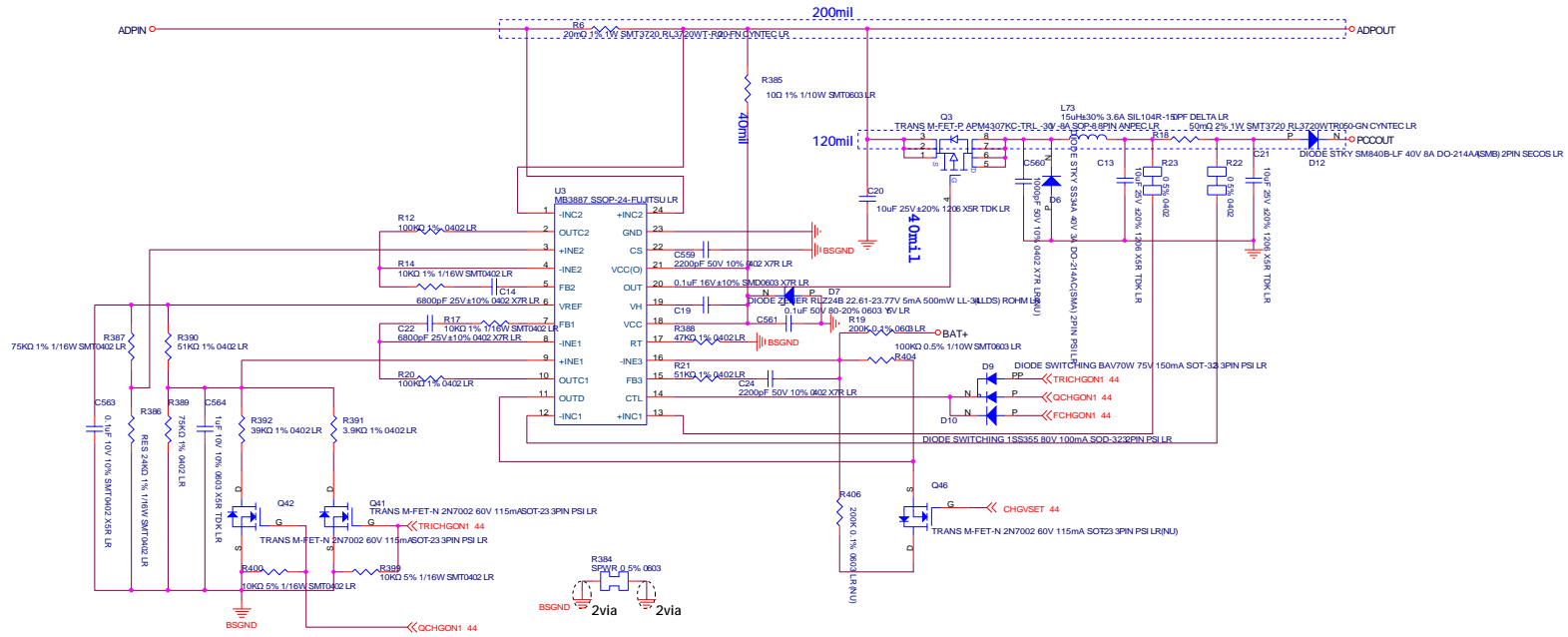


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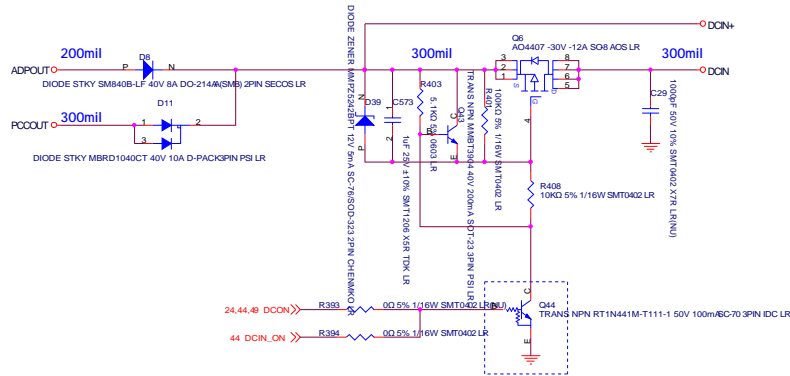
File		MR040T-Merom+Crestline GM965+ICH8M	
Size		Adaptor in & Battery Voltage Sense	
Date		Monday, July 30, 2007	
Sheet		47 of 56	



# Charger



# DCIN

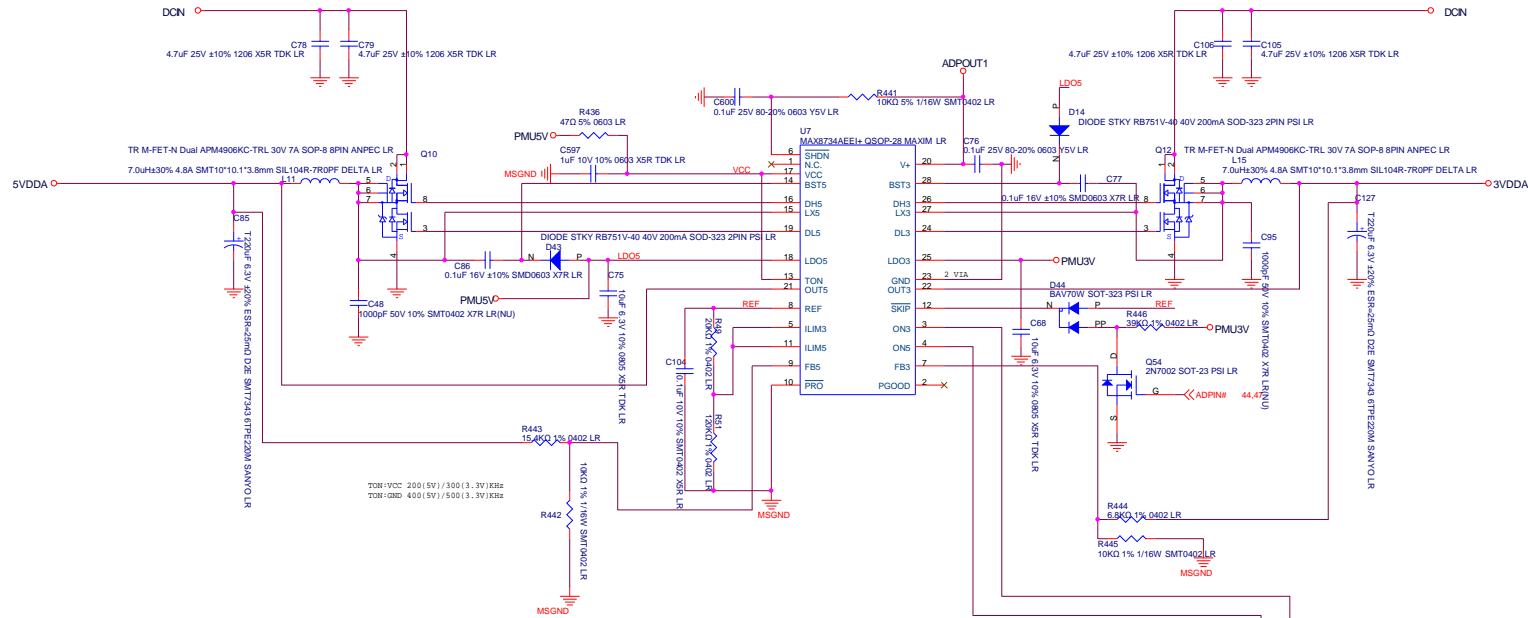


- 44, 47 BAT+ ○ BAT+
- 47 DCIN+ ○ DCIN+
- 27, 46, 47, 49, 50, 9, 52 DCIN ○ DCIN
- 47 PCCOUT ○ PCCOUT
- 47 ADP/N ○ ADP/N
- 47 ADP/N ○ ADP/N

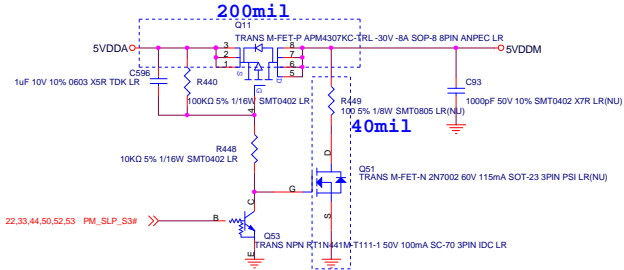
		<b>First International Computer, Inc.</b> 5FL NO.300, Yang Guang St. Ntshu 114 TAIPEI, TAIWAN, ROC (886-2)8751-8751	
File		<b>Confidential</b>	
<b>MR040T&gt;Merom+CreStire GM965+CH8M</b>			
Size	Document Number	Rev	0.4
Customer	<b>Charger Circuit /DCIN</b>		
Date:	Monday, July 30, 2007	Sheet	48 of 56



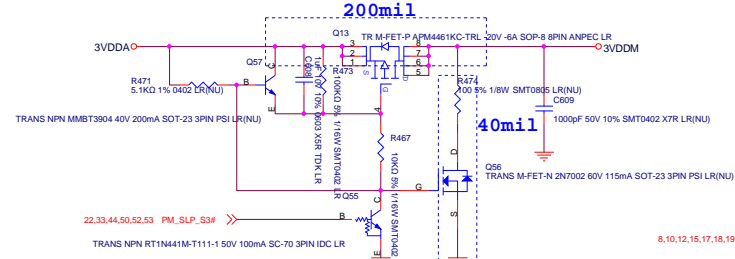
# 5VDDA/S/M, 3VDDA/S/M



## 5VDDS/5VDDM



## 3VDDS/3VDDM

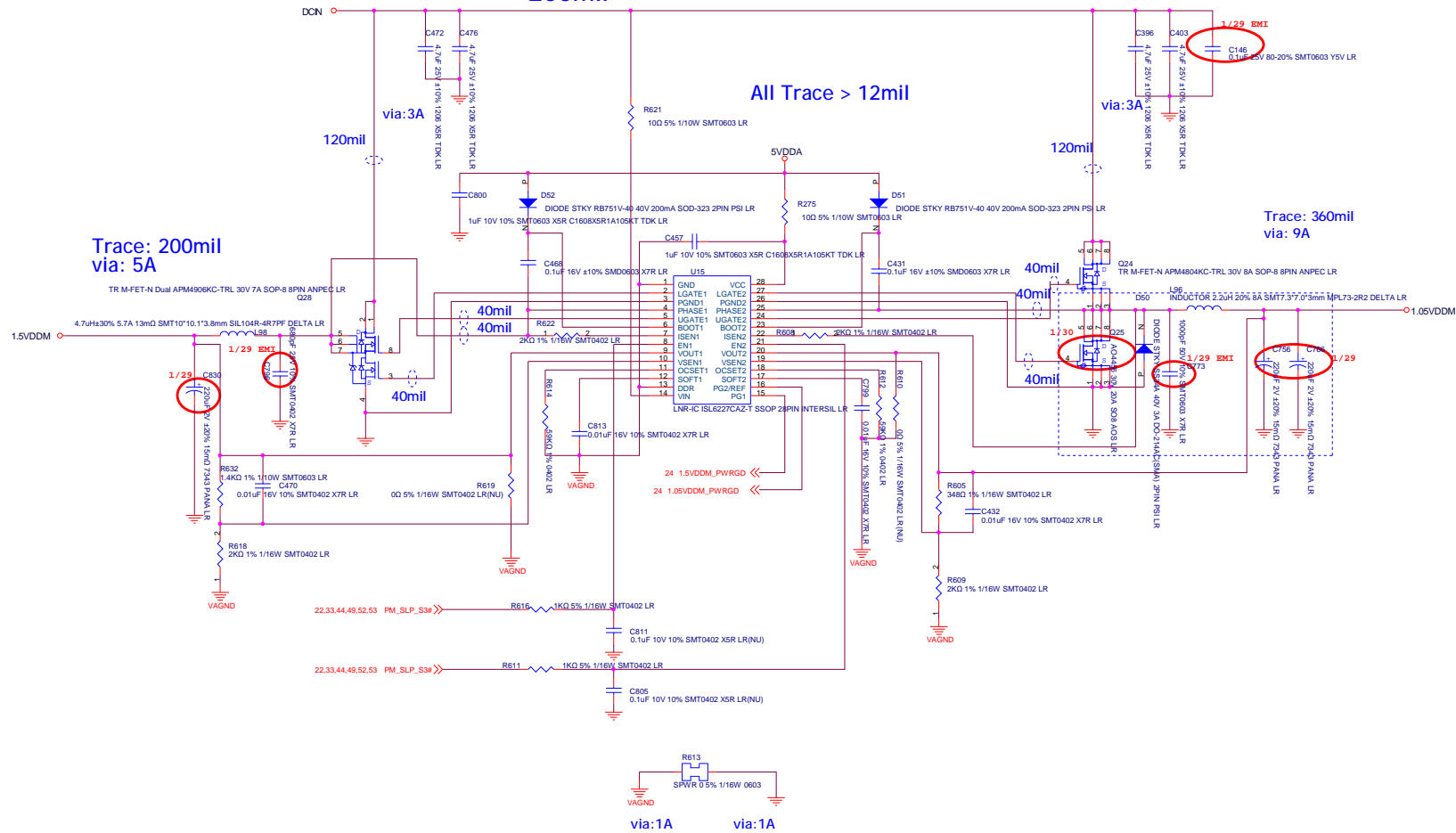


21,44,47	PMU5V	PMU5V
30,44	PMU5V	PMU5V
10,20,21,22,23,24,26,27,29,33,34,35,42,43,44,47,51	3VDDA	3VDDA
10,23,28,29,31,40,41	5VDDM	5VDDM
23,30,32,34,43,46,50,51,52,53	5VDDA	5VDDA
47	ADPOUT1	ADPOUT1
27,46,47,48,50,51,52	DCIN	DCIN
8,10,12,15,17,18,19,20,21,22,23,24,26,27,28,29,30,31,33,35,37,38,39,42,43,44,46,52,53	3VDDM	3VDDM

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<b>Confidential</b>		
Title	MR040T>Merom+Creline GM965+CH8M	
Size	Document Number	Rev
C	3/5VDDA/S/M, PMU3/5V	0.4
Date	Monday, July 30, 2007	Sheet 49 of 56



Trace: 360mil  
via: 9A



9,14,15,20,21,23,42,43 1.5VDDM ○ 1.5VDDM

8,9,11,14,15,17,21,23 1.05VDDM ○ 1.05VDDM

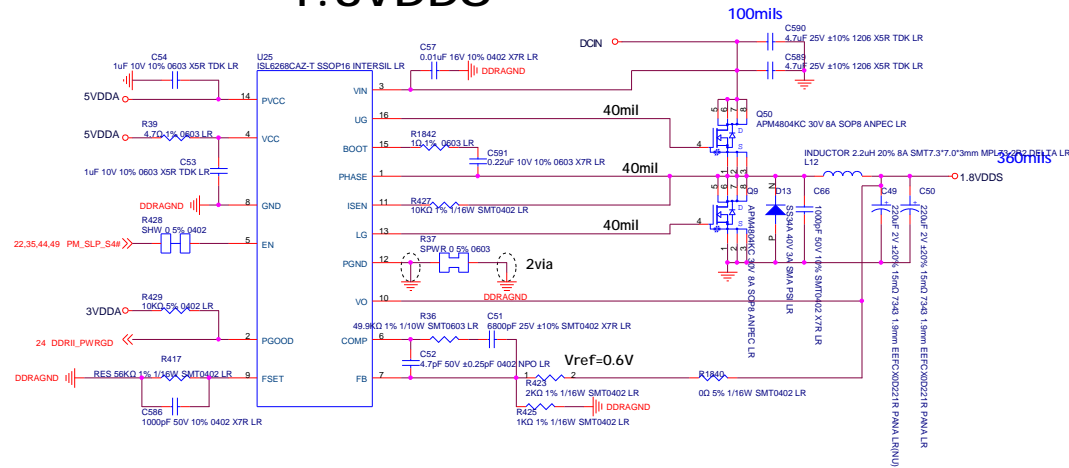
10,20,21,22,23,24,26,27,29,33,34,35,42,43,44,47,49,51 3VDDA  3VDDA

23,30,32,34,43,46,49,51,52,53 5VDDA ○ 5VDDA

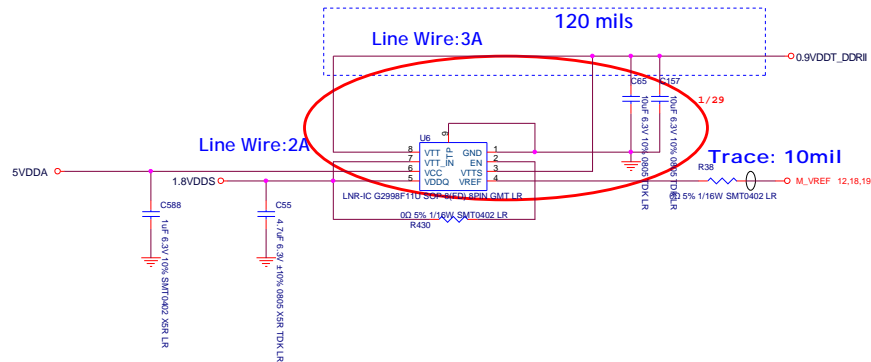
27,46,47,48,49,51,52 DCIN  DCIN




1.8VDDS



## DDRII Terminator Power

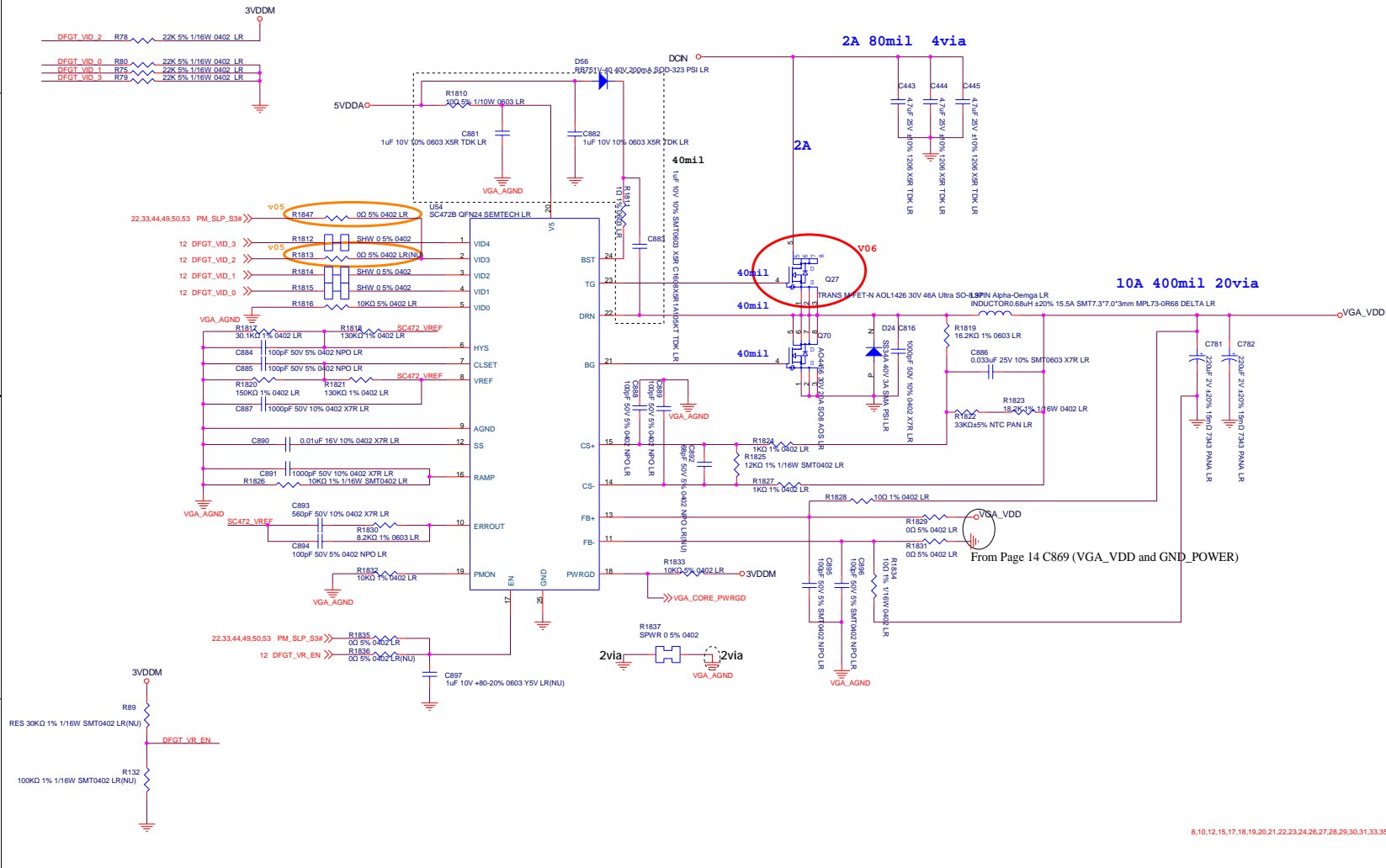


12,18,19 M\_VREF 0 M\_VREF  
18,19 0.9VDDT\_DORII 0.9VDDT\_DORII  
12,14,15,18,19,53 1.8VDDS 1.8VDDS  
10,20,21,22,23,24,26,27,29,33,34,35,42,43,44,47,49 3VDDA 3VDDA  
23,30,32,34,43,46,49,50,52,53 5VDDA 5VDDA  
27,46,47,48,49,50,52 DCIN DCIN

 <b>First International Computer, Inc.</b> SFL No.300, Yang Guang St., NeiHu 114 TAIPEI, TAIWAN, R.O.C. (886-2)8751-6751		<b>Confidential</b>
Title <b>MR040T&gt;Merom+Crestline GM965+CH8M</b>		
Size C	Document Number <b>DDR Power</b>	Rev 0.4
Date: Monday, July 30, 2007 Sheet 51 of 56		



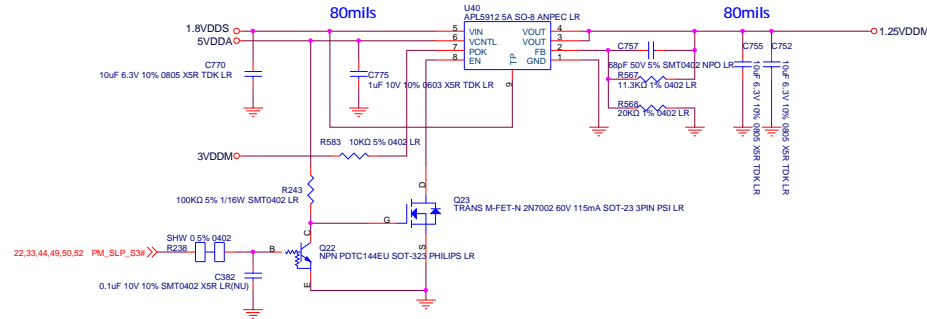
# VGACORE (Santa Rosa)



8,10,12,15,17,18,19,20,21,22,23,24,26,27,28,29,30,31,33,35,37,38,39,42,43,44,46,49,53 14 VGA\_VDD 3VDDM 5VDDA DCIN



# 1.25VDDM



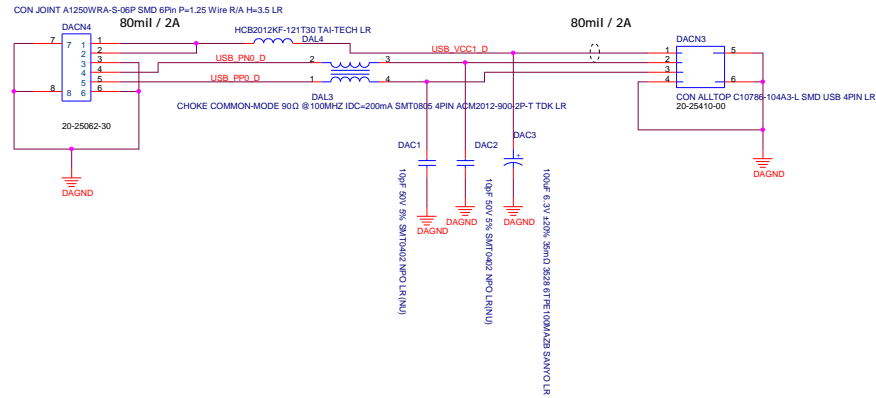
10,20,21,22,23,24,26,27,29,33,34,35,42,43,44,47,49,51	3VDDA	3VDDA
8,10,12,15,17,18,19,20,21,22,23,24,26,27,28,29,30,31,33,35,37,38,39,42,43,44,46,49,52	3VDDM	3VDDM
12,14,15,18,19,51	1.8VDD5	1.8VDD5
23,30,32,34,43,46,49,50,51,52	5VDDA	5VDDA
12,15,17,23	1.25VDDM	1.25VDDM

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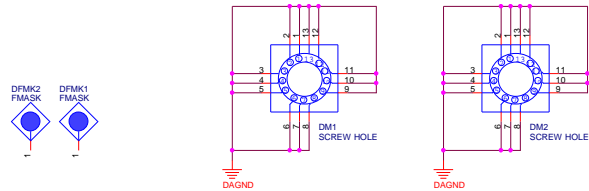
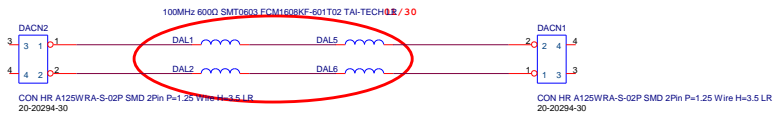
Title			MR040T>Merom+Crestline GM965+ICH8M
Size	Document Number	Rev	0.4
C	VGADDR 1.8V 2.5V		
Date	Monday, July 30, 2007	Sheet	53 of 56



# MR040T USB Board

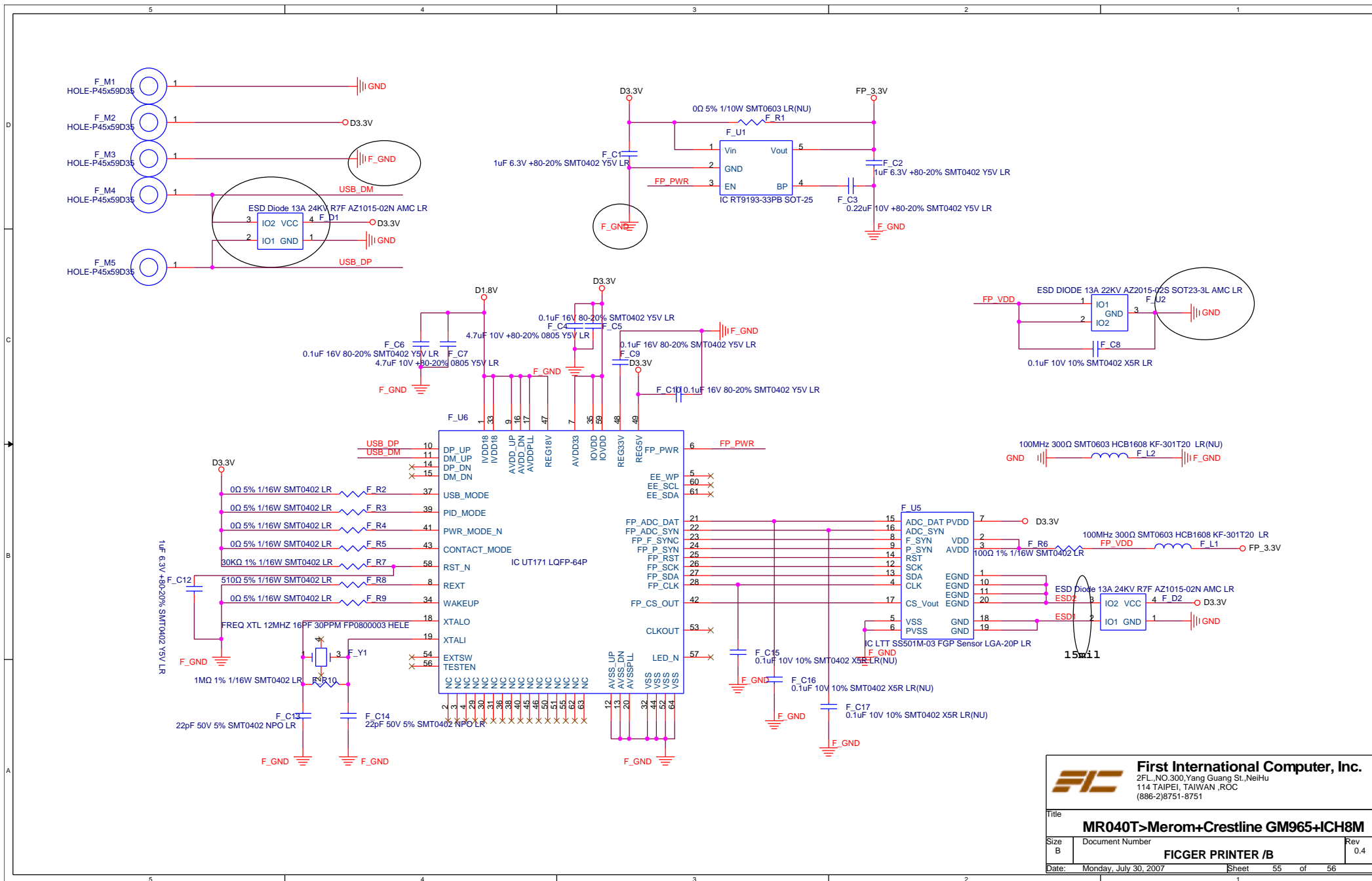


For MDC modem



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<b>MR040T&gt;Merom+Crestline GM965+CH8M</b>		
Size	Document Number	Rev
C	VR240T (Yonah + VIA VN896 + VT8237A)	0.4
Date:	Monday, July 30, 2007	Sheet 54 of 56





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Title  
**MR040T>Merom+Crestline GM965+ICH8M**

Size  
B

Date:  
Monday, July 30, 2007

Document Number  
**FICGER PRINTER /B**

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Rev  
0.4



**MR040T from ES/WS to TR (Rev0.2->0.3) HR**

**MR040T from TR to PP (Rev0.3->0.4)PIR**

Item	Reason for change	PAGE	Modify List	MB. Ver.	Date
1	PMX can't drive PM_RSMRST# to 3.3V(Only 2V)	22	N.I. R273 <del>PU-PM_RSMRST# to 3VDDA with R289</del>	0.3	11/29
2	For BIOS debugging purpose	32	Connect CN12 to USB port 1 Connect CN7 to USB port 0	0.3	11/30
3	Modify 1.8VDD5 OCP porint	51	Modify R427 from 2K $\Omega$ to 10K $\Omega$	0.3	12/04
4	<del>Modify LOM PCIe pairs from port 6 to port 5</del>	20	Add CB41,C835 <del>Reserve R85,R135,R136,R137</del>	0.3	12/11
5	Modify USB differential pair's inductor to common mode choke	32	Del L13, L14, L9, L10, L18, L19 Add L105, L106, L107	0.3	12/15
6	Co-lay maxiam thermal sensor	10	Add U55	0.3	12/15
7	Update SPI ROM P/N	26		0.3	12/15
8	Modify Giga LAN chip version to B0	35		0.3	12/15
9	Add two jumper for shorting DGND and AGND For EMI request.	40	Add R320, R321	0.3	12/26
10	Remove duplicate PU resistor for KBCSCI#	44	Del R520	0.3	12/26
11	Remove reserved cap, the n modified to common mode choke at LVDS differential pair.	27	Remove footprint C522, C521, C529, C530, C528, C527, C523  Add L108, L109, L110, L111	0.3	12/26

	<b>First International Computer, Inc.</b> 5FL NO.383, Yang Guo S1, Nanshu 114 TAIPEI, TAIWAN, ROC (886-2)8751-8751
Title <b>MR040T+Merom+Crestline GM965+CH8M</b>	Document Number
Size C	<b>MR040T+Merom+Crestline GM965+CH8M</b>
Date: Monday, July 30, 2007	Sheet 56 of 56